THE DINI GROUP

User Manual

DNMEG_ARM_TILE (REV2)

LOGIC EMULATION SOURCE

DNMEG_ARM_TILE (REV2) User Manual
Version 2.0

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Chapter 1

Introduction

This User Manual accompanies the DNMEG_ARM_TILE (REV2) Daughter Card. For specific information regarding the Spartan part, please reference the datasheet on the Xilinx website.

1 About the DNMEG_ARM_TILE Daughter Card

The DNMEG_ARM_TILE (REV2) Daughter Card provides a development platform for designing and verifying applications targeted for use with an ARM processor. This board provides designers access to commonly used peripherals and full utility of the ARM processor on a connected Core Tile. The DNMEG_ARM_TILE (REV2) Daughter Card can operate in standalone mode or in conjunction with one of the Dini products that houses a 400 pin MEG-Array Daughter card header, e.g. DN7020k10.

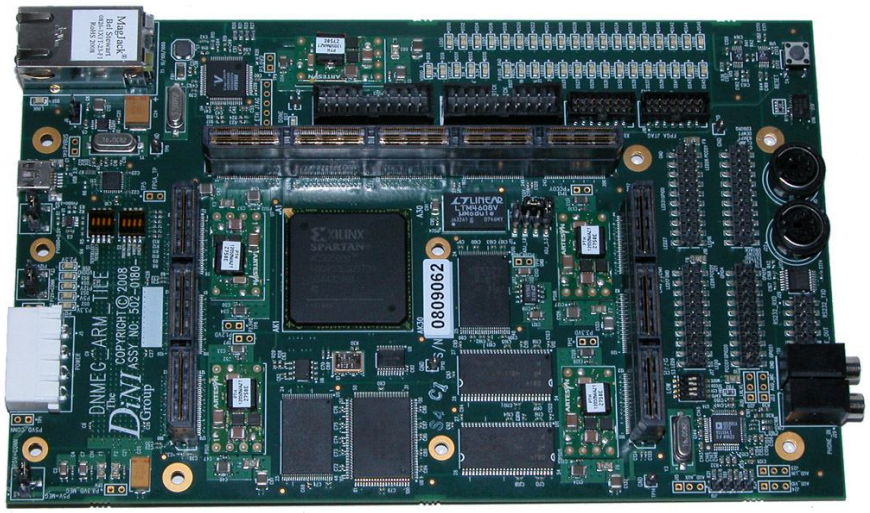


Figure 1 - DNMEG_ARM_TILE (REV2) Daughter Card

2 DNMEG_ARM_TILE (REV2) Daughter Card Features

DNMEG_ARM_TILE (REV2) Daughter Card features the following:

- AHB Interface
    - The AHB interface from the ARM Core Tile is connected both to the on-board Spartan FPGA and to the MEG-Array connector. This allows for standalone usage, base-board only usage, or a combination of base-board and on-board FPGA usage.
    - Sample RTL code is provided to give each peripheral on the DNMEG_ARM_TILE (REV2) an AHB interface, making the peripherals easily accessible from the ARM processor.
- Microprocessor Peripherals
    - Xilinx Spartan 3 FPGA (3S5000-S)
    - SDRAM – PC100/PC133: 16M x 32
    - SSRAM: 512K x 36
    - FLASH: 2M x 16
    - AC97 Audio
    - Keyboard/Mouse
    - RS232
    - Ethernet PHY – not available with DN7020k10 or DN9000k10
- Flexible Clock Resources
    - AHB clock can be generated using Spartan and on-board 100 MHz clock, or from base-board. This allows for AHB frequencies from 1-100 MHz.
    - Can use HCLK, Global Clock, retimed or delay-matched clocks for clocking Core Tile.
- FPGA Configuration

  - On-board Xilinx PROM for automatic configuration.
  - JTAG for configuration of Xilinx Spartan and PROM. Xilinx JTAG cable provided.

- ARM Configuration
  - Through a combination of switches and FPGA signals, all init and run-time configuration signals for the ARM processor can be programmed.
  - JTAG interface to the ARM Core Tile is provided, allowing third-party debuggers / emulators to communicate with the ARM processor.
- User LED's (x32)
- General Purpose I/O headers
- Onboard distributed Power Supplies
- MEG-Array (400 pin) interface to Dinigroup base-boards
- Full support for embedded Logic Analyzers
  - ChipScope™ Pro Analyzer
- RS232 Port, 10 pin Header – MicroBlaze Applications
- Stand Alone operation, requires an external +12V/+5V ATX power supply

3 Package Contents:

Before using the kit or installing the software, be sure to check the contents of the kit and inspect the board to verify that you received all of the items. If any of these items are missing, contact The Dini Group before you proceed. The DNMEG_ARM_TILE (REV2) Daughter Card kit includes the following:

- RS232 IDC Header to Female DB9 Cable Assembly
- RS232 Serial Cable Assembly, 6ft, F/F (DB9)
- CD ROM containing:
  - Spartan Reference Design (Verilog)

- User Manual (pdf format)
- Schematic (pdf format)
- Component Datasheets (pdf format)

Optional items that support development efforts (not provided):

- ü Xilinx ISE software and Xilinx Platform Cable USB download cable
- ü ARM debugging cable / emulator (JTAG)

4 Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. Verify that all components are on the board and appear intact.

5 Additional Information

For additional information, please visit http://www.dinigroup.com/. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Table 1 – Additional Information

Resource	Description / URL
User Manual	This is the main source of technical information. The manual should contain most of the answers to your questions
Demonstration Videos	MEG-Array Daughter Card header insertion and removal video
Dini Group Web Site	The web page will contain the latest user manual, application notes, FAQ, articles, and any device errata and manual addenda. Please visit and bookmark: http://www.dinigroup.com
Spartan 3 User Guide	Pages from Spartan 3 User Guide, which contains device-specific information on Xilinx device characteristics
ARM Core Tile Datasheet	Information about the ARM Core Tile, found here: http://www.arm.com/miscPDFs/7843.pdf
AMBA AHB Specification	A description of the signals on the AHB bus, found here: http://www.arm.com/products/solutions/AMBA_Spec.html

Resource	Description / URL
E-Mail	You may direct questions and feedback to the Dini Group using this e-mail address: support@dinigroup.com
Phone Support	Call us at **858.454.3419** during the hours of 10:00am to 5:00pm Pacific Time.
FAQ	The download section of the web page may contain a document called **DNMEG_ARM_TILE (REV2) Frequently Asked Questions (FAQ)**. This document is periodically updated with information that may not be in the User's Manual.

Chapter

2

Getting Started

Congratulations on your purchase of the DNMEG_ARM_TILE (REV2) Daughter Card. The remainder of this chapter describes how to start using the board.

1 Before You Begin

1.1 Configuring the Programmable Components

The DNMEG_ARM_TILE (REV2) Daughter Card has been factory tested and pre-programmed to ensure correct operation. The user does not need to alter any jumpers or program anything to see the board work.

1.2 Warnings

- **Connecting to the ARM Core Tile –** There are many different build options for the Core Tile, some of which involve resistor links between voltage sources. In order to prevent electrical damage to both the Core Tile and the DNMEG_ARM_TILE (REV2), please read the section on Core Tile preparation before mating the cards.

- **Daughter Card Test Headers (Over Voltage)** - The 400-pin daughter card test headers are **NOT** 5V tolerant. Take care when handling the board to avoid touching the components and daughter card connections due to ESD.

- **ESD Warning** - The board is sensitive to static electricity, so treat the PCB accordingly. The target markets for this product are engineers that are familiar with FPGAs and circuit boards. However, if needed, the following web page has an excellent tutorial on the "Fundamentals of ESD" for those of you who are new to ESD sensitive products:

  http://www.esda.org/basics/part1.cfm

- **Operating Temperature** - Avoid touching the PTH012050WAZ power supply modules (PSU1, PSU2, PSU3, PSU5, PSU6) as they operate at high temperatures and may cause skin burns.

2 Preparing the ARM Core Tile

2.1 Why is this Necessary?

The ARM core tile has many different stuffing options, and must be customized to fit a specific application. Our primary concern is the power connections that are, by default, installed on the tile. R25 and R182 connect PVDDIO (AHB signal voltage) on the Core Tile to 3.3V – we want to use our selectable on-board voltage of 2.5V or 3.0V to comply with the electrical limits of modern FPGAs. R24 and R183 connect PCCOY (expandable memory voltage) to 3.3V – we want to select from a variety of voltage ranges on the DNMEG_ARM_TILE (REV2) for compliance with a wider range of memory modules.

2.2 Removing Resistors

R25, R182, R24, and R183 need to be removed from the ARM Core Tile. Locations of these resistors are indicated below.

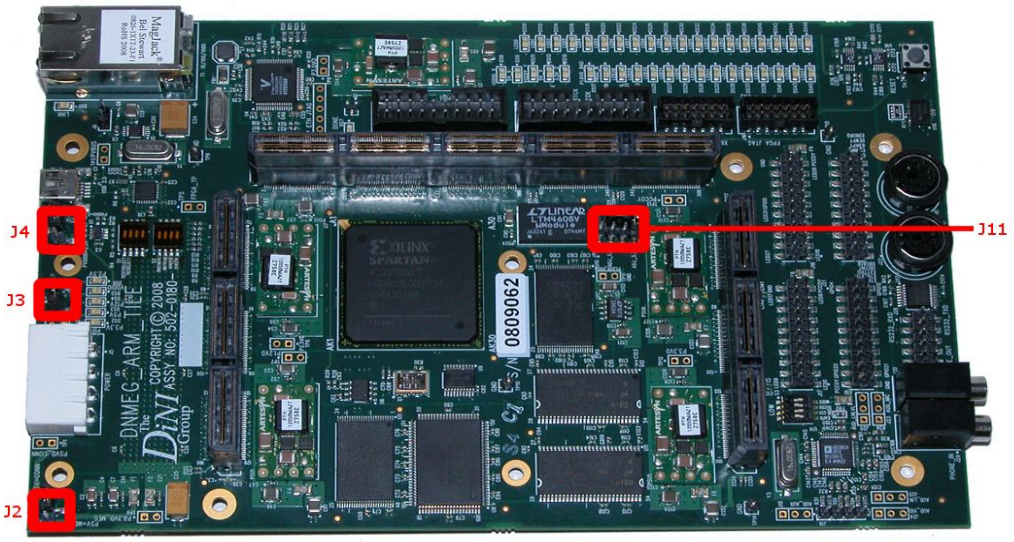
3 Preparing the DNMEG_ARM_TILE (REV2)

3.1 Power Options / Jumper Settings

The preferred method for powering the DNMEG_ARM_TILE (REV2) is through the ATX power connector J5. Jumper settings are available to power the board using a host board's supply through the Meg-Array connector. Jumpers are also available to change the voltage for the AHB and Memory Expansion signals to the Core Tile. Jumpers will installed at the factory before shipping – only change these settings if necessary.

Table 2 – Jumper Settings

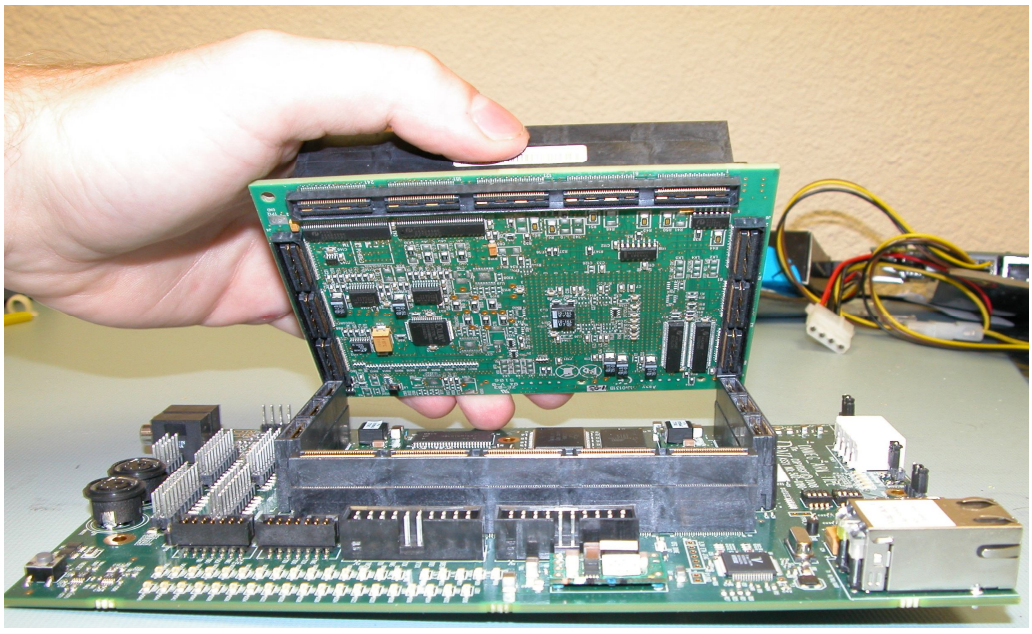
Jumper	Purpose
J2	Install Jumper on pins 2-3 to use 5V power from the ATX connector. Install on pins 1-2 to use 5V power from the Meg-Array.
J3	Install Jumper on pins 2-3 to use 12V power from the ATX connector. Install on pins 1-2 to use 12V power from the Meg-Array.
J4	Install Jumper on pins 1-2 to use 3V as the VDDIO voltage for the AHB Bus. Install on pins 2-3 to use 2.5V.
J11	Leave all jumpers uninstalled for 1.2V Memory Expansion. Install jumper on pins 2-4 for 1.5V. Install jumper on pins 3-4 for 1.8V. Install jumper on pins 4-6 for 2.5V. Install jumpers on pins 4-6, 7-8 for 3.3V.



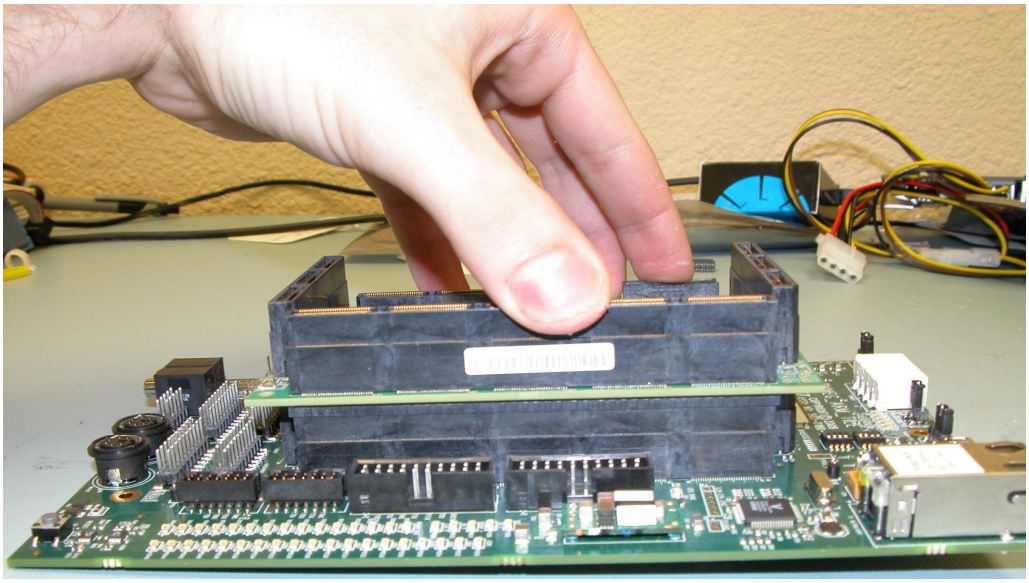
4 Mating the DNMEG_ARM_TILE (REV2) with the ARM Core Tile

4.1 Aligning the Headers

Begin by resting the far edge of the two horizontal headers on the ARM Core Tile on headers J7 and J14 on DNMEG_ARM_TILE (REV2).



While keeping the far edge aligned, allow the ARM Core Tile to lay flat on top of the DNMEG_ARM_TILE (REV2). The headers should be aligned.



4.2 Press Down Firmly

Press down firmly on each of the three ARM headers. Especially when dealing with new ARM Core Tiles, these connectors can be stiff. Firmly pressing each segment of each header is recommended.

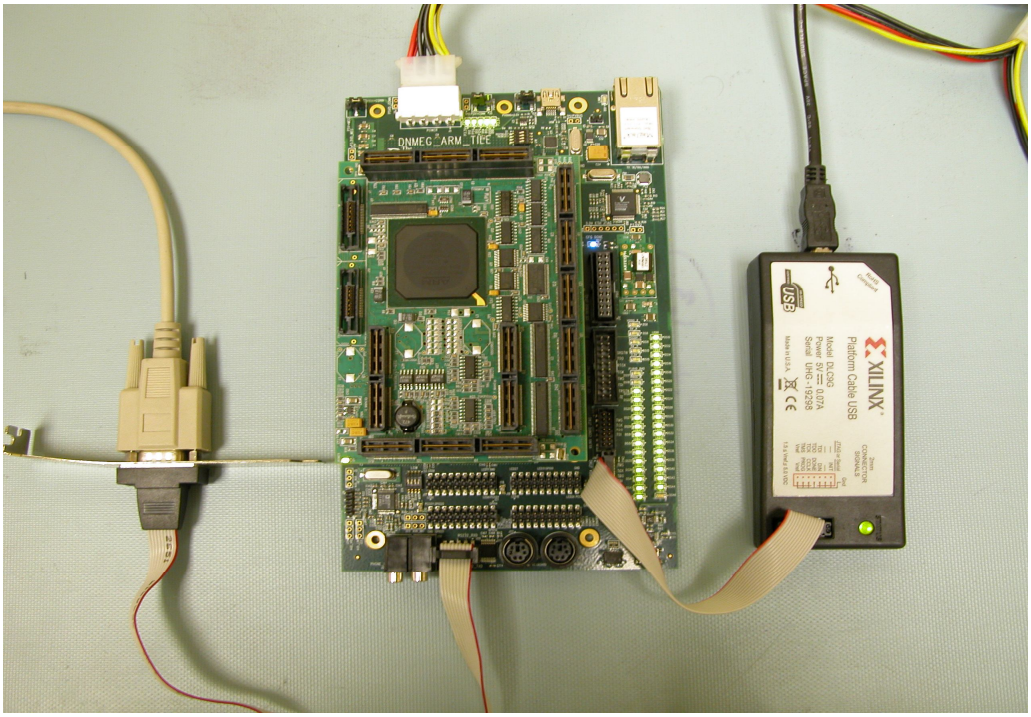
5 Using the Reference Design

The Dini Group provides reference designs for the DNMEG_ARM_TILE (REV2) to help the user get started with building applications:

- Reference – Loaded onto the board before shipped, allows for AHB communication.
- Loopback – Allows for testing of DNMEG_ARM_TILE (REV2) peripherals excluding AHB communication. Extra test cables are required (and not included) to test AHB and Meg-Array headers.

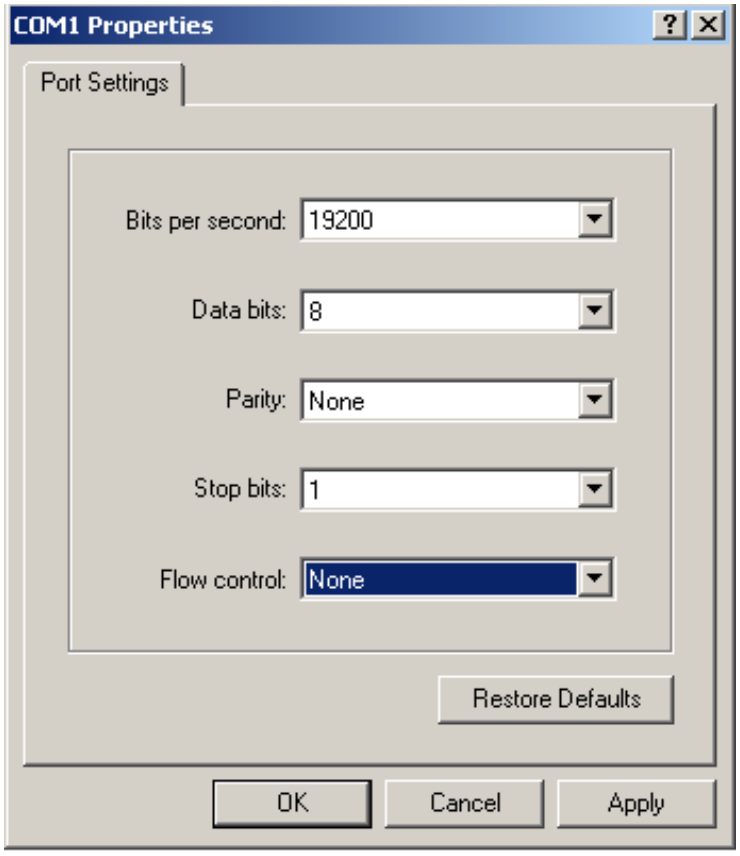
5.1 Initial Setup before Applying Power

Attach the ATX Power Supply to the power header (J5) on the DNMEG_ARM_TILE (REV2) Daughter Card. Connect the "Xilinx Platform Cable USB" from the Test PC to the JTAG header (J16). Connect the serial cable from the Test PC to the RS232 header (J26). Ensure that pin 1 location of the cable aligns with pin 1 location on the PCB.



5.2 Serial COM Setup using Hyperterminal

Connect the RS232 Serial cable to a COM port on the host computer and the RS232 header (J26) on the DNMEG_ARM_TILE (REV2) Daughter Card. Configure Hyperterminal to the following settings:



Warning: The text in the buffer window (the window above the command window) may appear to be corrupted. The text in the command window should move to the buffer window as the text scrolls past the top line in the command window. However, the text may appear in the buffer window with missing characters or extra characters. See Microsoft Help and Support, article ID: 274261

5.3 Running the Reference Design

Once the board powers on, it will load the bitfile stored in the Xilinx PROM and come out of reset. The attached ARM Core Tile will begin to execute the code stored in the FLASH on the DNMEG_ARM_TILE (REV2). When shipped, the code in the FLASH will toggle the LEDs on the DNMEG_ARM_TILE (REV2). If desired, AHB transactions can be initiated over RS232 by sending command files. See the reference design README for further details.

In order to execute code from the FLASH, some configuration signals must be set in a certain way, described as follows:

Table 3 – Reference Design Configuration Signals

Signal Name	Pin	Switch State	Signal State
XHEADER_BIGENDIN	S2.1	OFF	HIGH
XHEADER_INITRAM	S2.2	ON	LOW
XHEADER_VINITHI	S2.3	ON	LOW

5.4 Running the Loopback Design

Power-Up the DNMEG_ARM_TILE (REV2) Daughter Card and program the Spartan FPGA with the loopback bitfile. See the section on programming the Spartan FPGA for further detail. Open a Hyperterminal Window and view the output of the design. The loopback design will run read/write tests on SRAM, DRAM, AHB headers, and Meg-Array headers. It will also echo RS232 input and PS/2 Keyboard/Mouse input to the RS232 terminal, and detect when an ARM Core Tile is attached. Because loopback cables are not provided for the AHB headers and Meg-Array header, errors for these tests will occur. This is a diagnostic test only for testing interfaces to the DNMEG_ARM_TILE (REV2) peripherals.

5.5 Resetting a Design

Once a design is loaded, there are several ways to reset the design. If running standalone mode, reloading the design with iMPACT is an easy way to do so. The reset button S4 is a "hard" reset, and will cause the FPGA to reload from the PROM. If running attached to a host board, the reset sent across the MEG-Array connector can be used as a "soft"reset, meaning that it will reset the logic of the FPGA without reconfiguring it.

Chapter 3

Programming/Configuring the Hardware

This chapter details the programming and configuration instructions for the DNMEG_ARM_TILE (REV2) Daughter Card.

6 Introduction

Spartan 3 devices are configured by loading application-specific configuration data—the bitstream—into internal memory. Because Xilinx FPGA configuration memory is volatile, it must be configured each time it is powered-up. The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes (the following configuration options are supported on this board):

- JTAG/Boundary-Scan
- Master-Serial from on-board Xilinx PROM

7 Configuration Options

This section lists detailed instructions for programming the Xilinx Virtex-5 FPGA using iMPACT, Version 10.1 tools. Before configuring the FPGA, ensure that the Xilinx software and the "Xilinx Platform Cable USB" driver software are installed on the host computer.

Note: This User Manual will not be updated for every revision of the Xilinx ISE tools, so please be aware of minor differences.

7.1 Configuring the FPGA using JTAG

The JTAG/Boundary-Scan configuration interface is always available, regardless of the Mode pin settings. The JTAG/Boundary-Scan configuration mode disables all other configuration modes to prevent conflicts between configuration interfaces.

7.1.1 Setup

Before configuring the FPGA, ensure the following steps have been completed:

1. Attach an ATX Power Supply to the Power header (J5) on the DNMEG_ARM_TILE (REV2) Daughter Card.

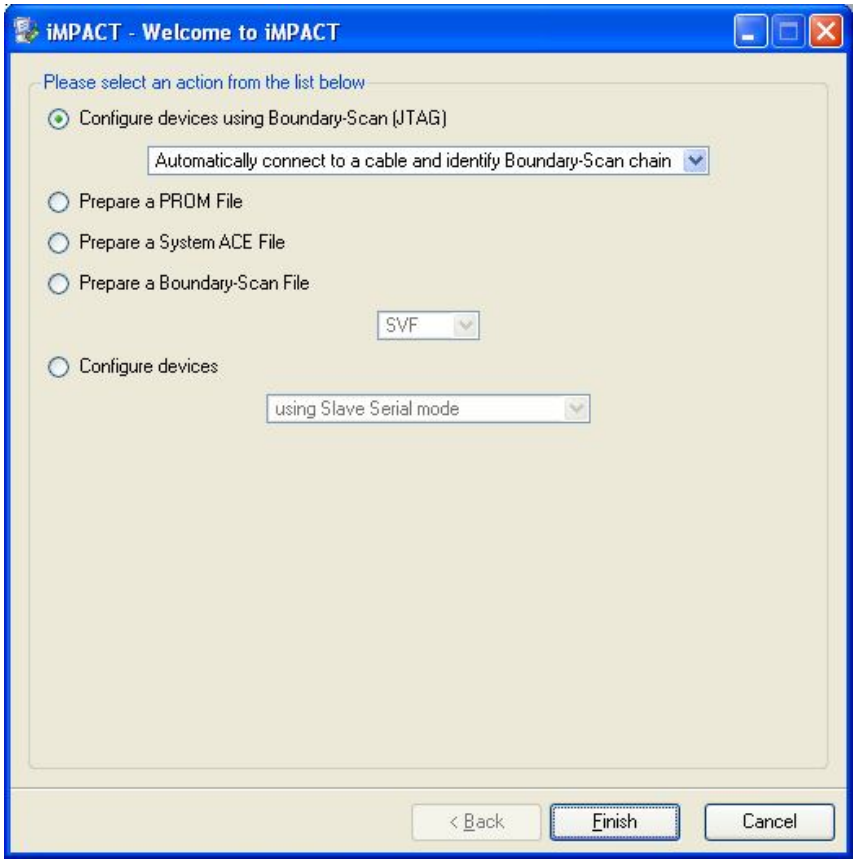
2. Connect the "Xilinx Platform Cable USB" to the "FPGA JTAG" header (J16).

3. Power up the board by turning ON the ATX power supply and verify that the Power LEDs DS2-DS6 are ON indicating adequate power supply.

7.1.2 Configuring the FPGA

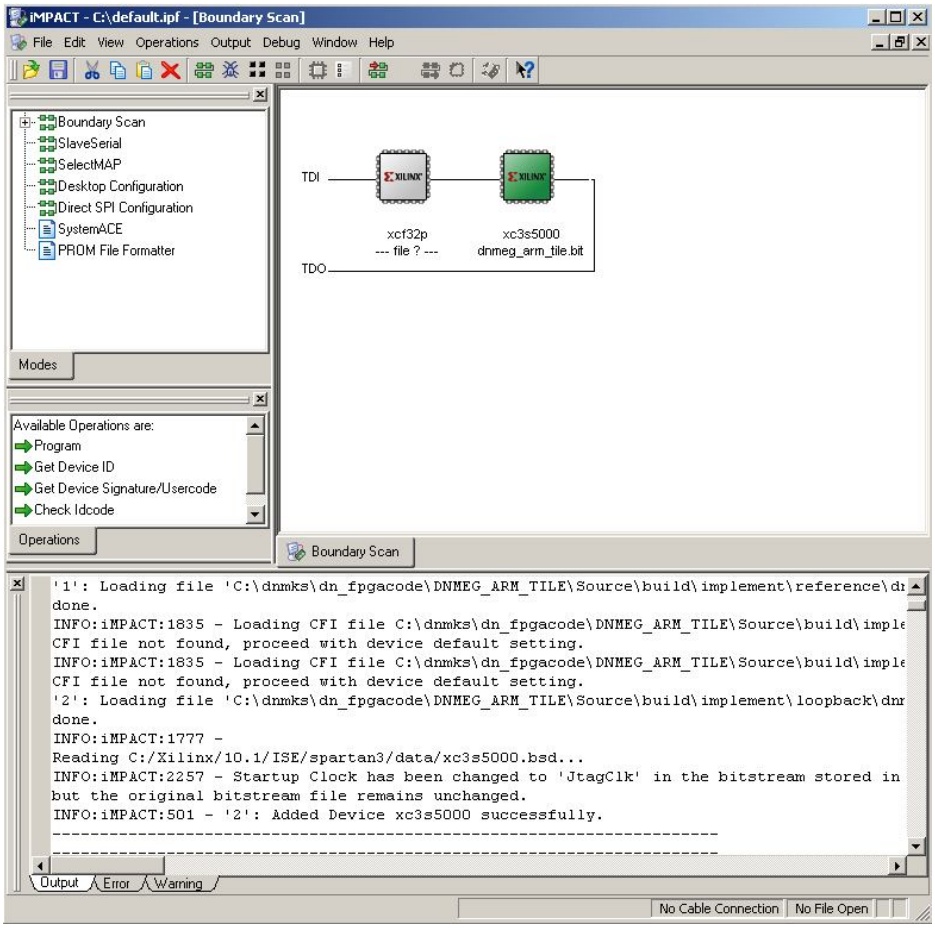
To configure the Xilinx FPGA, perform the following steps:

1. Open iMPACT and create a new default project. Select "**Configure devices using Boundary-Scan (JTAG)**" from the iMPACT welcome menu.



2. iMPACT will identify the PROM (XCF32P) and the FPGA (XC3S5000) in the JTAG chain. A pop-up window will display "**Assign New Configuration File**". Click "**Bypass**" and specify the location for the FPGA bit file;

   Select Device 2 in the "**Device Programming Properties**" window and click "**OK**" to continue.



3. Right-click on the FPGA and select the "**Program**" option. A "Progress Dialog" box will appear indicating programming progress.

4. The activation of the "CFG DONE" blue LED (DS7) indicates that the FPGA configured successfully.

7.2 Configuring the FPGA using Xilinx PROM

The Master-Serial mode is designed so that the FPGA can be configured from a Xilinx Flash PROM. The DNMEG_ARM_TILE (REV2) Daughter Card is populated with an XCF32P, 32Mbit Flash PROM.

7.2.1 Setup

Before configuring the FPGA, ensure the following steps have been completed:

1. Attach an ATX Power Supply to the Power header (J31) on the DNMEG_ARM_TILE (REV2) Daughter Card.

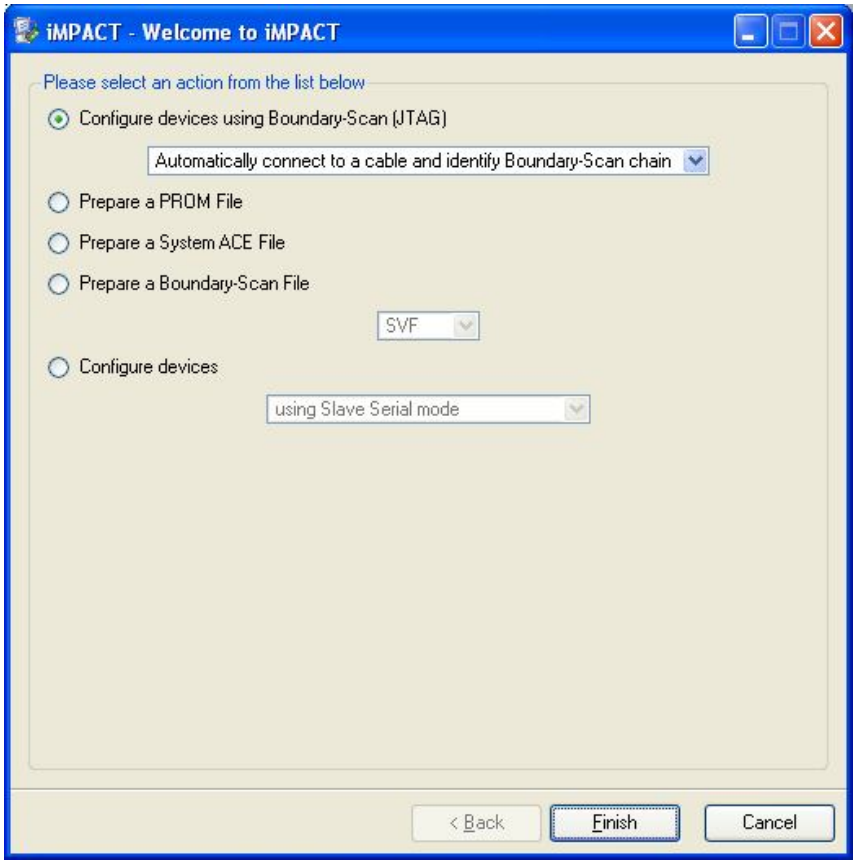
2. Connect the "Xilinx Platform Cable USB" to the "JTAG" header (J2).

3. Power up the board by turning ON the ATX power supply and verify that the Power LEDs DS2-DS6 are ON indicating adequate power supply.

7.2.2 Configuring the FPGA

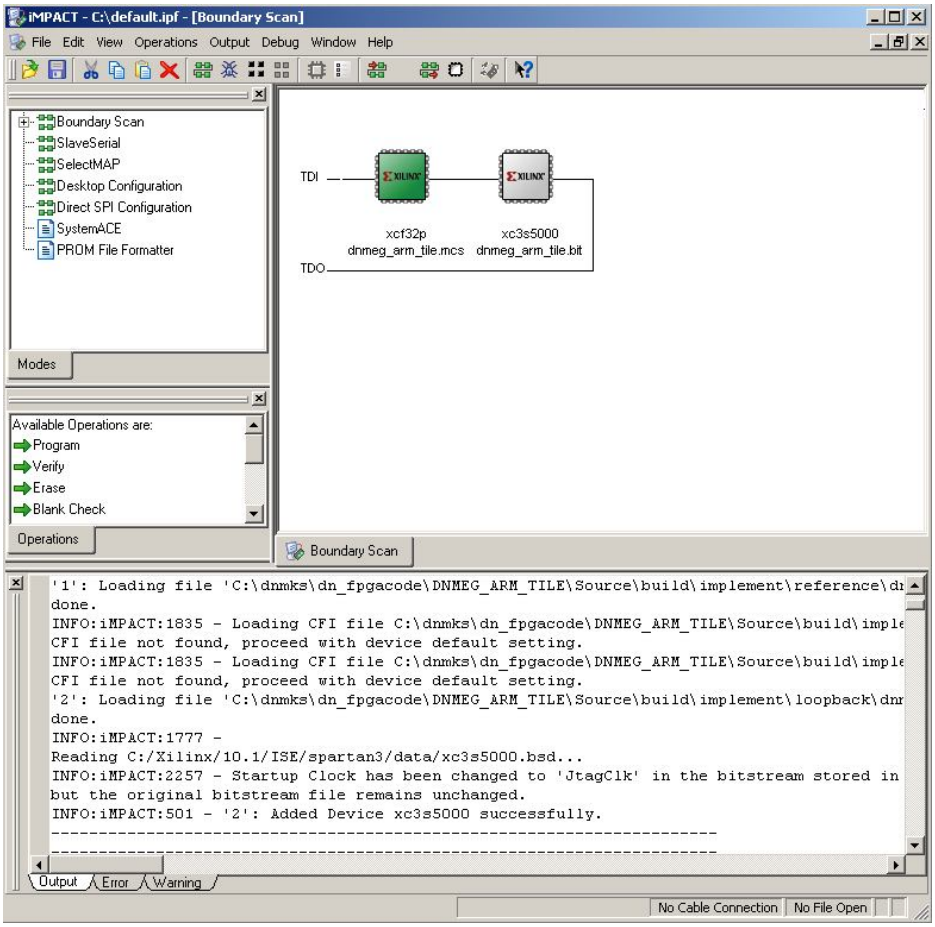
To configure the Xilinx Flash PROM, perform the following steps:

1. Open iMPACT and create a new default project. Select "**Configure devices using Boundary-Scan (JTAG)**" from the iMPACT welcome menu.



2. iMPACT will identify the PROM (XCF32P) and the FPGA (XC3S5000) in the JTAG chain. A pop-up window will display "**Assign New Configuration File**". Specify the PROM file location.

Select "**Bypass**" for the FPGA and click "**OK**" in the "Device Programming Properties" window to continue.



3. Right-click on the XCF32P device and select "**Program**". A Process Dialog box will indicate programming progress.

4. Power-cycle the DNMEG_ARM_TILE (REV2) Daughter Card or hit Reset Button S4 and verify that the "FPGA DONE" blue LED (DS7) is enabled, indicating successful configuration of the FPGA.

Chapter

4

Hardware Description

This chapter describes the functional blocks of the design and focuses on the Hardware.

8 Overview

The DNMEG_ARM_TILE (REV2) Daughter Card provides for a comprehensive collection of peripherals to use in creating a system around the Xilinx Spartan 3 FPGA. A high level block diagram of the DNMEG_ARM_TILE (REV2) Daughter Card is shown in Figure 2, followed by a brief description of each section.

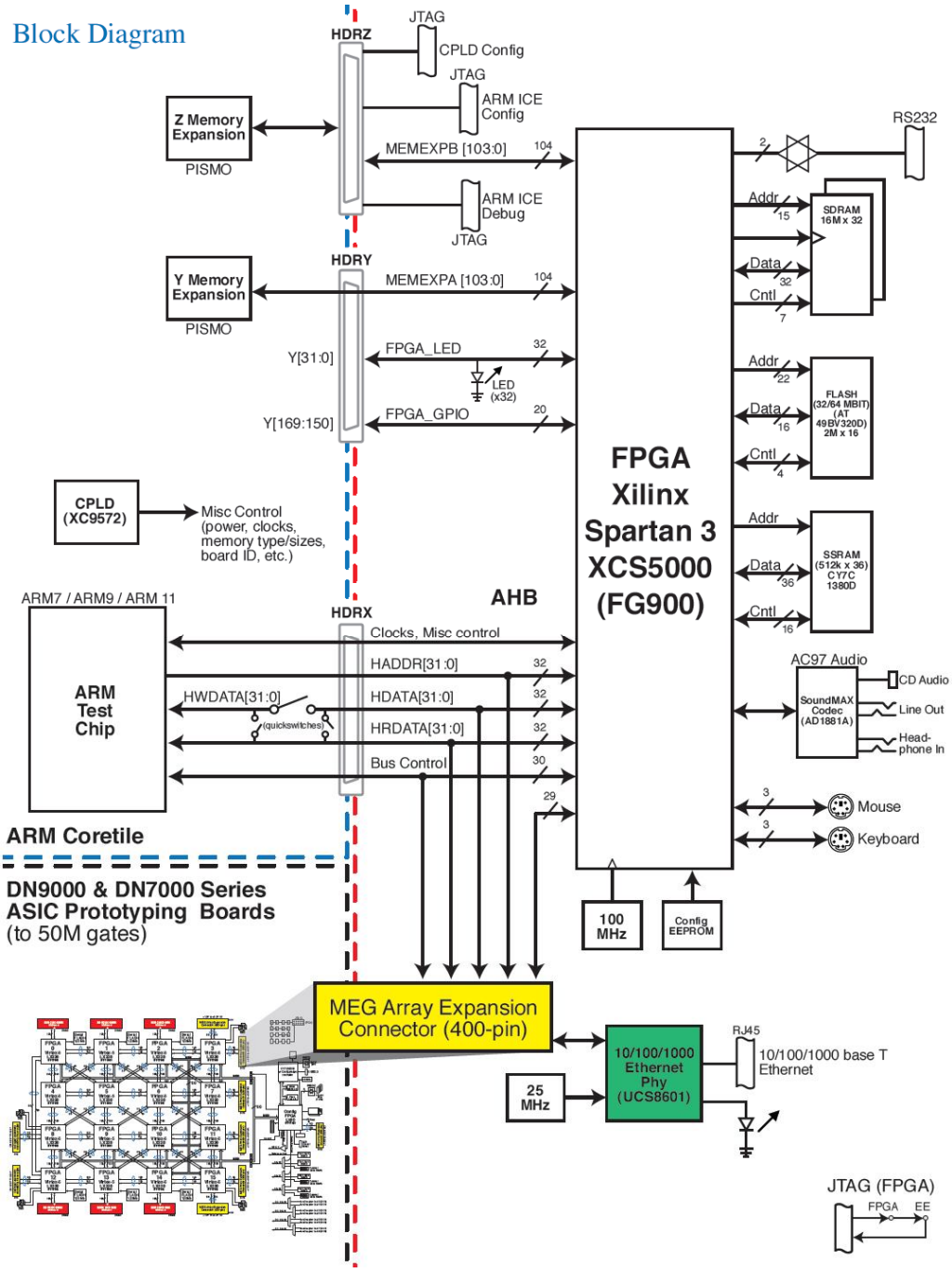


Figure 2 - DNMEG_ARM_TILE (REV2) Daughter Card Block Diagram

ARM supplies a circuit board with a processor test chip that has an ARM9 (or ARM11) within. ARM calls this product a RealView® Coretile. The DNMEG_ARM_TILE (REV2) is an intermediate host for a CoreTile adding the features and interfaces needed to make the ARM processor on the CoreTile useful for prototyping. The combination of the DNMEG_ARM_TILE (REV2) with the CoreTile is mounted on

an ASIC FPGA board from The DINI Group, enabling full speed system prototyping and debug of high gate count ARM-based systems. With a separate power supply, the DNMEG_ARM_TILE (REV2)/CoreTile combo can be used stand alone.

The CoreTile for ARM926EJ-S, for example, contains an ARM926EJ-S processor inside a test chip. The ARM9 processor's configuration signals and a multiplexed AHB bus are connected to the board's headers (HDRX). This CoreTile is mounted onto the DNMEG_ARM_TILE (REV2), which is, in turn, mounted onto any of the ASIC prototyping boards available from the DINI Group.

The AHB bus from HDRX is connected to the Spartan-3 FPGA and the 400-pin MEG_Array expansion header.

Memory expansion via PISMO is enabled to the CoreTile via HDRY. The Spartan-3 FPGA connects to most signals on this connector. User-controllable LEDs (32 in total) and 20 general purpose I/Os (GPIO) are also connected to the FPGA and HDRY.

Additional memory expansion via PISMO is enabled to the CoreTile via HDRZ. The Spartan-3 FPGA also connects to all signals on this header. The DNMEG_ARM_TILE (REV2) provides the proper connector for the variety of ARM in-circuit-emulators (ICE) and debug equipment via ARM ICE debug port.

9 Xilinx Spartan 3 FPGA

On the **DNMEG_ARM_TILE (REV2)** the AHB bus from the ARM processor is connected to a Xilinx Spartan-3 FPGA. The standard stuffing options is the 3S5000-4. All resources of this Xilinx FPGA are available to the user application. This is a fairly large FPGA, containing 66,560 FF/LUT pairs and 240kbytes of block RAM. By a conservative measure this FPGA alone can prototype 560k ASIC gates excluding memory and multipliers. This ASIC gate number can be increased in the short term to as much as 50M ASIC gates via a DN7020k10. When Altera releases the Stratix-4 family, this number will increase to >100M gates.

10 Peripherals

The intention of the DNMEG_ARM_TILE (REV2) is to provide AHB interfaces to useful peripherals common to most designs. Verilog source is provided for each of the interfaces, and allows the interface to be mapped into ARM address space for use by the processor on the Core Tile.

10.1 SDRAM – PC100/PC133

Two Micron synchronous DRAMS (MT48LC16M16A2) are connected to the FPGA in a 16M x 32 configuration. These SDRAMS are PC100/PC133 compliant.

10.2 SSRAM

A single Cypress pipelined SSRAM is connected to the FPGA in a 512k x 36 configuration.

10.3 FLASH

A single 32 megabit FLASH memory from Atmel is connected to the FPGA in a 2M x 16 configuration. Non-volatile memory and ARM instructions can be stored in the FLASH and read out by the ARM processor.

10.4 AC97 Audio

An Analog Devices AD1881A is connected to the FPGA. A CD Audio, Line Out, and Headphone IN connector is provided. The AD1881A meets the *Audio Codec '97 2.0 and 2.1 Extensions*. In addition, the AD1881A SoundMAX Codec is designed to meet all requirements of the *Audio Codec '97, Component Specification,* Revision 1.03. The AD1881A also includes some other Codec enhanced features such as the built-in PHAT Stereo 3D enhancement.

10.5 Ethernet PHY - 10/100/1000base-T (not available with DN7020k10 or DN9000k10)

With an appropriate MAC, a Vitesse VSC8601 Ethernet PHY provides 10/100/1000base-T Ethernet.

11 Clock Generation

11.1 Clock Methodology

The DNMEG_ARM_TILE (REV2) has a flexible and configurable clocking scheme. Figure 3 is a block diagram showing the clocking resources and connections.

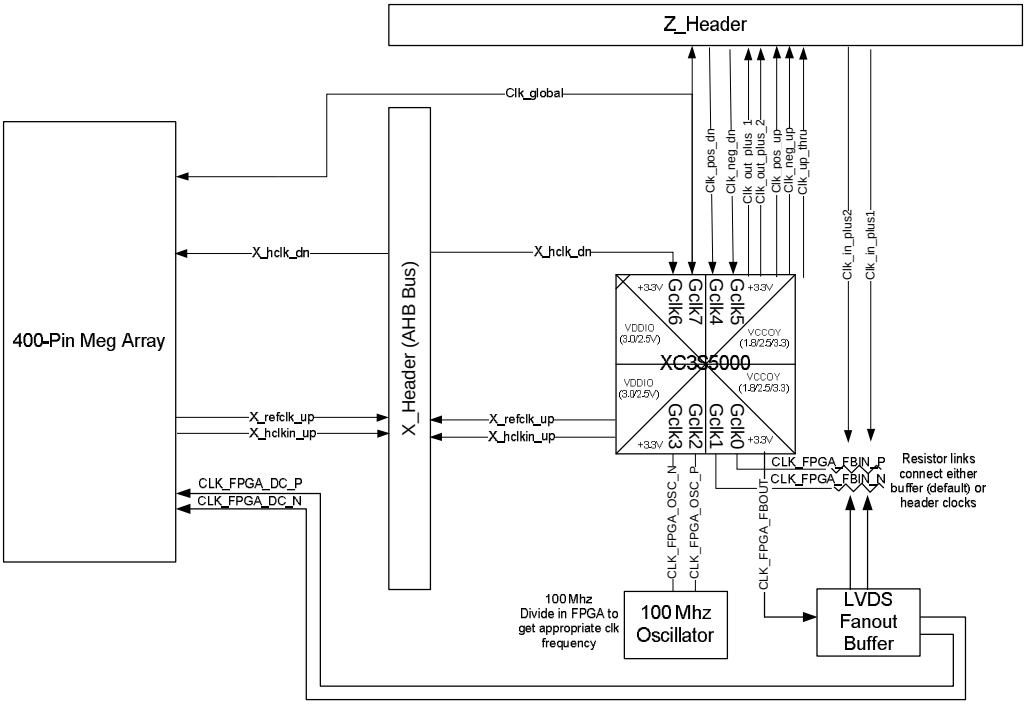


Figure 3 - Clocking Block Diagram

The clocking structures for the DNMEG_ARM_TILE (REV2) include the following features:

- 100 MHz Oscillator (X1)
- LVDS Fanout Buffer (U6) for system-synchronous operation between host-board and DNMEG_ARM_TILE (REV2)
- Support for both delay-matched and retimed clocks to/from the ARM Core Tile
- ARM Core Tile Global Clock support
- Ability to clock AHB standalone, from DNMEG_ARM_TILE (REV2) w/ host-board attached, or from host-board

The connections between the FPGA and various clocking resources are documented in Table 4.

Table 4 – FPGA Clocking

Signal Name	FPGA Pin	Function
CLK_FPGA_OSC_P	U7.AH15	100 MHz from the Oscillator
CLK_FPGA_OSC_N	U7.AJ15	100 MHz from the Oscillator
CLK_FPGA_FBOUT	U7.AF15	Output to clock buffer for system-synchronous operation
CLK_FPGA_FBIN_P	U7.B16	Input from system-synchronous clock buffer
CLK_FPGA_FBIN_N	U7.C16	Input from system-synchronous clock buffer
XHEADER_REFCLK_UP	U7.L4	Output to ARM for use as AHB hclk input (on selected Core Tiles)
XHEADER_HCLKIN_UP	U7.L3	Output to ARM for use as AHB hclk input (on selected Core Tiles)
XHEADER_HCLK_DN	U7.A15	Input for clocking AHB interface
ZHEADER_CLK_GLOBAL	U7.B15	Output to ARM for use as AHB hclk input (on selected Core Tiles)
ZHEADER_CLK_POS_DN_IN	U7.AK16	Retimed clock – see ARM Core Tile documentation
ZHEADER_CLK_NEG_DN_IN	U7.AJ16	Retimed clock – see ARM Core Tile documentation
ZHEADER_CLK_POS_UP_OUT	U7.J22	Retimed clock – see ARM Core Tile documentation
ZHEADER_CLK_NEG_UP_OUT	U7.H22	Retimed clock – see ARM Core Tile documentation
ZHEADER_CLK_OUT_PLUS1	U7.F22	Delay-matched clock – see ARM Core Tile documentation
ZHEADER_CLK_OUT_PLUS2	U7.E22	Delay-matched clock – see ARM Core Tile documentation
ZHEADER_CLK_IN_PLUS1	U7.B16	Delay-matched clock – see ARM Core Tile documentation
ZHEADER_CLK_IN_PLUS2	U7.C16	Delay-matched clock – see ARM Core Tile documentation

11.2 Daughter Card Clocks

The 400 pin MEG-Array connector on the bottom of the PCBA is used to interface to the Dini Group products, e.g. DN7002k10MEG.

11.2.1 Connections between the FPGA and the Daughter Card Header Clocks

The connections between the FPGA and the Daughter Card Header Clocks are shown in Table 5.

Table 5 - Connections for Daughter Card Header Clocks

Signal Name	DC Pin	Function
XHEADER_HCLK_DN_2.5V	P1.E1	Input for clocking AHB interface
XHEADER_REFCLK_UP_2.5V	P1.F1	Output to ARM for use as AHB hclk input (on selected Core Tiles)
CLK_ETHB_RX_2.5V	P1.E3	Ethernet clock for receive data
ZHEADER_CLK_GLOBAL	P1.F3	Output to ARM for use as AHB hclk input (on selected Core Tiles)
CLK_FPGA_DC_P	P1.E5	Input from system-synchronous clock buffer
CLK_FPGA_DC_N	P1.F5	Input from system-synchronous clock buffer
XHEADER_HCLKIN_UP		Output to ARM for use as AHB hclk input (on selected Core Tiles)
CLK_ETHB_TX	P1.A37	Ethernet clock for transmit data
CLK125_ETHB	P1.K37	125 MHz Ethernet reference clock

12 ARM Headers

The ARM header (J7, J9, J14) connections were designed to be fully compliant with the CT926EJ-S featuring an ARM9 processor. For full descriptions of the function of these signals, please consult the ARM Core Tile documentation.

Table 6 – ARM Header Connections

Signal Name	FPGA Pin
XHEADER_ARM_PORESET_N	U7.W4
XHEADER_BIGENDOUT	U7.W7
XHEADER_CONFIGINIT	U7.W6
XHEADER_CONFIGRST_N	U7.W3
XHEADER_FIQ_N	U7.W9
XHEADER_HADDR0	U7.AA2
XHEADER_HADDR1	U7.AA3

Signal Name	FPGA Pin
XHEADER_HADDR10	U7.T2
XHEADER_HADDR11	U7.Y3
XHEADER_HADDR12	U7.Y4
XHEADER_HADDR13	U7.T7
XHEADER_HADDR14	U7.T8
XHEADER_HADDR15	U7.AB6
XHEADER_HADDR16	U7.J8
XHEADER_HADDR17	U7.K9
XHEADER_HADDR18	U7.K7
XHEADER_HADDR19	U7.K6
XHEADER_HADDR2	U7.Y10
XHEADER_HADDR20	U7.K3
XHEADER_HADDR21	U7.K2
XHEADER_HADDR22	U7.K10
XHEADER_HADDR23	U7.L10
XHEADER_HADDR24	U7.L8
XHEADER_HADDR25	U7.L7
XHEADER_HADDR26	U7.L6
XHEADER_HADDR27	U7.L5
XHEADER_HADDR28	U7.M5
XHEADER_HADDR29	U7.N6
XHEADER_HADDR3	U7.AA10
XHEADER_HADDR30	U7.N5
XHEADER_HADDR31	U7.N4
XHEADER_HADDR4	U7.Y7
XHEADER_HADDR5	U7.Y8
XHEADER_HADDR6	U7.Y5
XHEADER_HADDR7	U7.Y6
XHEADER_HADDR8	U7.T4
XHEADER_HADDR9	U7.T1
XHEADER_HBURST0	U7.V1
XHEADER_HBURST1	U7.V5
XHEADER_HBURST2	U7.V4
XHEADER_HBUSREQ	U7.V6
XHEADER_HCLKIN_UP	U7.L3
XHEADER_HDATA0	U7.AH1
XHEADER_HDATA1	U7.AH2
XHEADER_HDATA10	U7.AE2
XHEADER_HDATA11	U7.AE3
XHEADER_HDATA12	U7.AD3
XHEADER_HDATA13	U7.AD4
XHEADER_HDATA14	U7.AD1

Signal Name	FPGA Pin
XHEADER_HDATA15	U7.AD2
XHEADER_HDATA16	U7.AC7
XHEADER_HDATA17	U7.AD6
XHEADER_HDATA18	U7.AC5
XHEADER_HDATA19	U7.AC6
XHEADER_HDATA2	U7.AG3
XHEADER_HDATA20	U7.AC3
XHEADER_HDATA21	U7.AC4
XHEADER_HDATA22	U7.AC1
XHEADER_HDATA23	U7.AC2
XHEADER_HDATA24	U7.AB4
XHEADER_HDATA25	U7.AB5
XHEADER_HDATA26	U7.AB1
XHEADER_HDATA27	U7.AB2
XHEADER_HDATA28	U7.AA9
XHEADER_HDATA29	U7.AB8
XHEADER_HDATA3	U7.AG4
XHEADER_HDATA30	U7.AA6
XHEADER_HDATA31	U7.AA7
XHEADER_HDATA4	U7.AG1
XHEADER_HDATA5	U7.AG2
XHEADER_HDATA6	U7.AF1
XHEADER_HDATA7	U7.AF2
XHEADER_HDATA8	U7.AE5
XHEADER_HDATA9	U7.AF4
XHEADER_HGRANT	U7.W10
XHEADER_HLOCK	U7.V9
XHEADER_HPROT0	U7.U3
XHEADER_HPROT1	U7.U2
XHEADER_HPROT2	U7.U7
XHEADER_HPROT3	U7.U6
XHEADER_HPROT4	U7.U10
XHEADER_HPROT5	U7.U9
XHEADER_HRDATA0	U7.M8
XHEADER_HRDATA1	U7.M9
XHEADER_HRDATA10	U7.R9
XHEADER_HRDATA11	U7.R10
XHEADER_HRDATA12	U7.P2
XHEADER_HRDATA13	U7.P3
XHEADER_HRDATA14	U7.P6
XHEADER_HRDATA15	U7.P7
XHEADER_HRDATA16	U7.P9

Signal Name	FPGA Pin
XHEADER_HRDATA17	U7.P10
XHEADER_HRDATA18	U7.N1
XHEADER_HRDATA19	U7.N2
XHEADER_HRDATA2	U7.R1
XHEADER_HRDATA20	U7.N8
XHEADER_HRDATA21	U7.N9
XHEADER_HRDATA22	U7.N10
XHEADER_HRDATA23	U7.M10
XHEADER_HRDATA24	U7.M1
XHEADER_HRDATA25	U7.M2
XHEADER_HRDATA26	U7.M3
XHEADER_HRDATA27	U7.M4
XHEADER_HRDATA28	U7.M6
XHEADER_HRDATA29	U7.M7
XHEADER_HRDATA3	U7.R2
XHEADER_HRDATA30	U7.L1
XHEADER_HRDATA31	U7.L2
XHEADER_HRDATA4	U7.R3
XHEADER_HRDATA5	U7.R4
XHEADER_HRDATA6	U7.R5
XHEADER_HRDATA7	U7.R6
XHEADER_HRDATA8	U7.R7
XHEADER_HRDATA9	U7.R8
XHEADER_HREADY	U7.V8
XHEADER_HRESP0	U7.V10
XHEADER_HRESP1	U7.W2
XHEADER_HRESP2	U7.W1
XHEADER_HSIZE0	U7.T5
XHEADER_HSIZE1	U7.T10
XHEADER_HSIZE2	U7.T9
XHEADER_HTRANS0	U7.T3
XHEADER_HTRANS1	U7.T6
XHEADER_HWRITE	U7.W5
XHEADER_IRQ_N	U7.W8
XHEADER_PLLLOCK	U7.Y1
XHEADER_REFCLK_UP	U7.L4
XHEADER_RESET_N	U7.Y2
XHEADER_PLLFBDIV0	U7.B27
XHEADER_PLLFBDIV1	U7.A27
XHEADER_PLLFBDIV2	U7.C27
XHEADER_PLLFBDIV3	U7.D26
XHEADER_PLLFBDIV4	U7.B26

Signal Name	FPGA Pin
XHEADER_PLLFBDIV5	U7.A26
XHEADER_PLLFBDIV6	U7.C25
XHEADER_PLLFBDIV7	U7.B25
XHEADER_PLLOUTDIV0	U7.F25
XHEADER_PLLOUTDIV1	U7.F24
XHEADER_PLLOUTDIV2	U7.D24
XHEADER_PLLOUTDIV3	U7.C24
XHEADER_PLLREFDIV0	U7.D23
XHEADER_PLLREFDIV1	U7.C23
XHEADER_PLLREFDIV2	U7.B23
XHEADER_PLLREFDIV3	U7.A23
XHEADER_HCLKDIV0	U7.G24
XHEADER_HCLKDIV1	U7.A24
XHEADER_HCLKDIV2	U7.B24
XHEADER_PLLBYPASS	U7.H23
XHEADER_PLLCTRL0	U7.G23
XHEADER_PLLCTRL1	U7.F23
XHEADER_HCLK_DN	U7.A15
YHEADER_MEMEXPA0	U7.J29
YHEADER_MEMEXPA1	U7.J30
YHEADER_MEMEXPA10	U7.G25
YHEADER_MEMEXPA100	U7.T22
YHEADER_MEMEXPA101	U7.T23
YHEADER_MEMEXPA102	U7.T24
YHEADER_MEMEXPA103	U7.T25
YHEADER_MEMEXPA11	U7.H24
YHEADER_MEMEXPA12	U7.G29
YHEADER_MEMEXPA13	U7.G30
YHEADER_MEMEXPA14	U7.G27
YHEADER_MEMEXPA15	U7.G28
YHEADER_MEMEXPA16	U7.F28
YHEADER_MEMEXPA17	U7.F29
YHEADER_MEMEXPA18	U7.E29
YHEADER_MEMEXPA19	U7.E30
YHEADER_MEMEXPA2	U7.J26
YHEADER_MEMEXPA20	U7.D29
YHEADER_MEMEXPA21	U7.D30
YHEADER_MEMEXPA22	U7.D27
YHEADER_MEMEXPA23	U7.D28
YHEADER_MEMEXPA24	U7.C29
YHEADER_MEMEXPA25	U7.C30
YHEADER_MEMEXPA26	U7.K22

Signal Name	FPGA Pin
YHEADER_MEMEXPA27	U7.J23
YHEADER_MEMEXPA28	U7.K25
YHEADER_MEMEXPA29	U7.K24
YHEADER_MEMEXPA3	U7.J27
YHEADER_MEMEXPA30	U7.L26
YHEADER_MEMEXPA31	U7.L25
YHEADER_MEMEXPA32	U7.L28
YHEADER_MEMEXPA33	U7.L27
YHEADER_MEMEXPA34	U7.L30
YHEADER_MEMEXPA35	U7.L29
YHEADER_MEMEXPA36	U7.M23
YHEADER_MEMEXPA37	U7.M22
YHEADER_MEMEXPA38	U7.M25
YHEADER_MEMEXPA39	U7.M24
YHEADER_MEMEXPA4	U7.H29
YHEADER_MEMEXPA40	U7.M28
YHEADER_MEMEXPA41	U7.M27
YHEADER_MEMEXPA42	U7.N21
YHEADER_MEMEXPA43	U7.M21
YHEADER_MEMEXPA44	U7.N23
YHEADER_MEMEXPA45	U7.N22
YHEADER_MEMEXPA46	U7.N25
YHEADER_MEMEXPA47	U7.M26
YHEADER_MEMEXPA48	U7.N27
YHEADER_MEMEXPA49	U7.N26
YHEADER_MEMEXPA5	U7.H30
YHEADER_MEMEXPA50	U7.N30
YHEADER_MEMEXPA51	U7.N29
YHEADER_MEMEXPA52	U7.P22
YHEADER_MEMEXPA53	U7.P21
YHEADER_MEMEXPA54	U7.P25
YHEADER_MEMEXPA55	U7.P24
YHEADER_MEMEXPA56	U7.P29
YHEADER_MEMEXPA57	U7.P28
YHEADER_MEMEXPA58	U7.R22
YHEADER_MEMEXPA59	U7.R21
YHEADER_MEMEXPA6	U7.H27
YHEADER_MEMEXPA60	U7.R24
YHEADER_MEMEXPA61	U7.R23
YHEADER_MEMEXPA62	U7.R26
YHEADER_MEMEXPA63	U7.R25
YHEADER_MEMEXPA64	U7.R28

Signal Name	FPGA Pin
YHEADER_MEMEXPA65	U7.R27
YHEADER_MEMEXPA66	U7.R30
YHEADER_MEMEXPA67	U7.R29
YHEADER_MEMEXPA68	U7.F26
YHEADER_MEMEXPA69	U7.E27
YHEADER_MEMEXPA7	U7.H28
YHEADER_MEMEXPA70	U7.K29
YHEADER_MEMEXPA71	U7.K28
YHEADER_MEMEXPA72	U7.L21
YHEADER_MEMEXPA73	U7.K21
YHEADER_MEMEXPA74	U7.L24
YHEADER_MEMEXPA75	U7.L23
YHEADER_MEMEXPA76	U7.M30
YHEADER_MEMEXPA77	U7.M29
YHEADER_MEMEXPA78	U7.J25
YHEADER_MEMEXPA79	U7.Y27
YHEADER_MEMEXPA8	U7.H25
YHEADER_MEMEXPA80	U7.Y28
YHEADER_MEMEXPA81	U7.Y29
YHEADER_MEMEXPA82	U7.Y30
YHEADER_MEMEXPA83	U7.W29
YHEADER_MEMEXPA84	U7.W30
YHEADER_MEMEXPA85	U7.W21
YHEADER_MEMEXPA86	U7.V21
YHEADER_MEMEXPA87	U7.V22
YHEADER_MEMEXPA88	U7.V23
YHEADER_MEMEXPA89	U7.W26
YHEADER_MEMEXPA9	U7.H26
YHEADER_MEMEXPA90	U7.V25
YHEADER_MEMEXPA91	U7.V29
YHEADER_MEMEXPA92	U7.V30
YHEADER_MEMEXPA93	U7.U21
YHEADER_MEMEXPA94	U7.U22
YHEADER_MEMEXPA95	U7.U24
YHEADER_MEMEXPA96	U7.U25
YHEADER_MEMEXPA97	U7.U28
YHEADER_MEMEXPA98	U7.U29
YHEADER_MEMEXPA99	U7.T21
ZHEADER_CFGEN_N	U7.J17
ZHEADER_CLK_GLOBAL	U7.B15
ZHEADER_CLK_NEG_DN_IN	U7.AJ16
ZHEADER_CLK_NEG_UP_OUT	U7.H22

Signal Name	FPGA Pin
ZHEADER_CLK_OUT_PLUS1	U7.F22
ZHEADER_CLK_OUT_PLUS2	U7.E22
ZHEADER_CLK_POS_DN_IN	U7.AK16
ZHEADER_CLK_POS_UP_OUT	U7.J22
ZHEADER_CLK_UP_THRU	U7.E23
ZHEADER_FPGA_IMAGE	U7.K20
ZHEADER_GLOBAL_DONE	U7.J21
ZHEADER_MEMEXPB0	U7.A4
ZHEADER_MEMEXPB1	U7.B4
ZHEADER_MEMEXPB10	U7.C7
ZHEADER_MEMEXPB100	U7.H18
ZHEADER_MEMEXPB101	U7.E18
ZHEADER_MEMEXPB102	U7.D18
ZHEADER_MEMEXPB103	U7.B18
ZHEADER_MEMEXPB11	U7.D7
ZHEADER_MEMEXPB12	U7.E8
ZHEADER_MEMEXPB13	U7.F8
ZHEADER_MEMEXPB14	U7.C8
ZHEADER_MEMEXPB15	U7.D8
ZHEADER_MEMEXPB16	U7.A8
ZHEADER_MEMEXPB17	U7.B8
ZHEADER_MEMEXPB18	U7.H9
ZHEADER_MEMEXPB19	U7.J9
ZHEADER_MEMEXPB2	U7.A5
ZHEADER_MEMEXPB20	U7.F10
ZHEADER_MEMEXPB21	U7.G10
ZHEADER_MEMEXPB22	U7.B10
ZHEADER_MEMEXPB23	U7.C10
ZHEADER_MEMEXPB24	U7.K11
ZHEADER_MEMEXPB25	U7.J10
ZHEADER_MEMEXPB26	U7.G11
ZHEADER_MEMEXPB27	U7.H11
ZHEADER_MEMEXPB28	U7.E11
ZHEADER_MEMEXPB29	U7.F11
ZHEADER_MEMEXPB3	U7.B5
ZHEADER_MEMEXPB30	U7.C11
ZHEADER_MEMEXPB31	U7.D11
ZHEADER_MEMEXPB32	U7.A11
ZHEADER_MEMEXPB33	U7.B11
ZHEADER_MEMEXPB34	U7.J12
ZHEADER_MEMEXPB35	U7.K12
ZHEADER_MEMEXPB36	U7.G12

Signal Name	FPGA Pin
ZHEADER_MEMEXPB37	U7.H12
ZHEADER_MEMEXPB38	U7.E12
ZHEADER_MEMEXPB39	U7.F12
ZHEADER_MEMEXPB4	U7.E6
ZHEADER_MEMEXPB40	U7.C12
ZHEADER_MEMEXPB41	U7.D12
ZHEADER_MEMEXPB42	U7.A12
ZHEADER_MEMEXPB43	U7.B12
ZHEADER_MEMEXPB44	U7.H13
ZHEADER_MEMEXPB45	U7.J13
ZHEADER_MEMEXPB46	U7.E13
ZHEADER_MEMEXPB47	U7.F13
ZHEADER_MEMEXPB48	U7.A13
ZHEADER_MEMEXPB49	U7.B13
ZHEADER_MEMEXPB5	U7.D5
ZHEADER_MEMEXPB50	U7.J14
ZHEADER_MEMEXPB51	U7.K14
ZHEADER_MEMEXPB52	U7.F14
ZHEADER_MEMEXPB53	U7.G14
ZHEADER_MEMEXPB54	U7.B14
ZHEADER_MEMEXPB55	U7.C14
ZHEADER_MEMEXPB56	U7.H15
ZHEADER_MEMEXPB57	U7.J15
ZHEADER_MEMEXPB58	U7.F15
ZHEADER_MEMEXPB59	U7.G15
ZHEADER_MEMEXPB6	U7.B6
ZHEADER_MEMEXPB60	U7.C15
ZHEADER_MEMEXPB61	U7.D15
ZHEADER_MEMEXPB62	U7.A7
ZHEADER_MEMEXPB63	U7.B7
ZHEADER_MEMEXPB64	U7.H8
ZHEADER_MEMEXPB65	U7.G7
ZHEADER_MEMEXPB66	U7.D9
ZHEADER_MEMEXPB67	U7.E9
ZHEADER_MEMEXPB68	U7.A9
ZHEADER_MEMEXPB69	U7.B9
ZHEADER_MEMEXPB7	U7.C6
ZHEADER_MEMEXPB70	U7.C4
ZHEADER_MEMEXPB71	U7.D13
ZHEADER_MEMEXPB72	U7.E15
ZHEADER_MEMEXPB73	U7.F9
ZHEADER_MEMEXPB74	U7.G8

Signal Name	FPGA Pin
ZHEADER_MEMEXPB75	U7.K13
ZHEADER_MEMEXPB76	U7.K15
ZHEADER_MEMEXPB77	U7.B20
ZHEADER_MEMEXPB78	U7.A20
ZHEADER_MEMEXPB79	U7.K19
ZHEADER_MEMEXPB8	U7.F7
ZHEADER_MEMEXPB80	U7.J19
ZHEADER_MEMEXPB81	U7.H19
ZHEADER_MEMEXPB82	U7.G19
ZHEADER_MEMEXPB83	U7.F19
ZHEADER_MEMEXPB84	U7.E19
ZHEADER_MEMEXPB85	U7.D19
ZHEADER_MEMEXPB86	U7.C19
ZHEADER_MEMEXPB87	U7.B19
ZHEADER_MEMEXPB88	U7.A19
ZHEADER_MEMEXPB89	U7.G17
ZHEADER_MEMEXPB9	U7.F6
ZHEADER_MEMEXPB90	U7.F17
ZHEADER_MEMEXPB91	U7.C17
ZHEADER_MEMEXPB92	U7.B17
ZHEADER_MEMEXPB93	U7.K16
ZHEADER_MEMEXPB94	U7.J16
ZHEADER_MEMEXPB95	U7.H16
ZHEADER_MEMEXPB96	U7.G16
ZHEADER_MEMEXPB97	U7.E16
ZHEADER_MEMEXPB98	U7.D16
ZHEADER_MEMEXPB99	U7.J18
ZHEADER_RTCKEN_N	U7.F16
ZHEADER_SPARE0	U7.D22
ZHEADER_SPARE1	U7.B22
ZHEADER_SPARE10	U7.E20
ZHEADER_SPARE11	U7.D20
ZHEADER_SPARE12	U7.C20
ZHEADER_SPARE2	U7.A22
ZHEADER_SPARE3	U7.G21
ZHEADER_SPARE4	U7.F21
ZHEADER_SPARE5	U7.C21
ZHEADER_SPARE6	U7.B21
ZHEADER_SPARE7	U7.H20
ZHEADER_SPARE8	U7.G20
ZHEADER_SPARE9	U7.F20
ZHEADER_SYSPOR_N	U7.A16

Signal Name	FPGA Pin
ZHEADER_SYSRST_N	U7.E25

In addition, several static signals are attached to DIP Switches S1 and S2. When the switches are in the OFF position, the signals will be HIGH. Turning the switches ON results in making the signals LOW.

Table 7 – Signals on S1 and S2

Signal Name	Pin
XHEADER_BIGENDIN	S2.1
XHEADER_INITRAM	S2.2
XHEADER_VINITHI	S2.3
XHEADER_DBGEN	S2.4
XHEADER_TESTSELECT	S1.1
XHEADER_TICSELECT	S1.2

13 General Purpose Headers

The FPGA_LED and FPGA_GPIO busses serve as general purpose communication, the FPGA_LED bus having the added bonus of being connected to LEDs. These busses are connected to the Spartan FPGA, the ARM Z Header, and surface mount headers for external interfacing.

Table 8 – General Purpose Headers

Signal Name	FPGA Pin	Header
FPGA_LED0	U7.AH29	J17.1
FPGA_LED1	U7.AH30	J17.3
FPGA_LED2	U7.AG27	J17.5
FPGA_LED3	U7.AG28	J17.7
FPGA_LED4	U7.AG29	J17.9
FPGA_LED5	U7.AG30	J17.11
FPGA_LED6	U7.AF29	J17.13
FPGA_LED7	U7.AF30	J17.15
FPGA_LED8	U7.AF27	J17.17
FPGA_LED9	U7.AE26	J17.2
FPGA_LED10	U7.AE28	J17.4
FPGA_LED11	U7.AE29	J17.6

Signal Name	FPGA Pin	Header
FPGA_LED12	U7.AD27	J17.8
FPGA_LED13	U7.AD28	J17.10
FPGA_LED14	U7.AD29	J17.12
FPGA_LED15	U7.AD30	J17.14
FPGA_LED16	U7.AD25	J17.16
FPGA_LED17	U7.AC24	J17.18
FPGA_LED18	U7.AC25	J18.1
FPGA_LED19	U7.AC26	J18.3
FPGA_LED20	U7.AC27	J18.5
FPGA_LED21	U7.AC28	J18.7
FPGA_LED22	U7.AC29	J18.9
FPGA_LED23	U7.AC30	J18.11
FPGA_LED24	U7.AB26	J18.13
FPGA_LED25	U7.AB27	J18.15
FPGA_LED26	U7.AB29	J18.17
FPGA_LED27	U7.AB30	J18.2
FPGA_LED28	U7.AB23	J18.4
FPGA_LED29	U7.AA22	J18.6
FPGA_LED30	U7.AA24	J18.8
FPGA_LED31	U7.AA25	J18.10
FPGA_GPIO0	U7.AA28	J18.12
FPGA_GPIO1	U7.AA29	J18.14
FPGA_GPIO2	U7.AA21	J18.16
FPGA_GPIO3	U7.Y21	J18.18
FPGA_GPIO4	U7.Y23	J21.1
FPGA_GPIO5	U7.Y23	J21.3
FPGA_GPIO6	U7.Y25	J21.5
FPGA_GPIO7	U7.Y26	J21.7
FPGA_GPIO8	U7.T26	J21.9
FPGA_GPIO9	U7.T27	J21.11
FPGA_GPIO10	U7.T28	J21.13
FPGA_GPIO11	U7.T29	J21.15
FPGA_GPIO12	U7.T30	J21.2

Signal Name	FPGA Pin	Header
FPGA_GPIO13	U7.W22	J21.4
FPGA_GPIO14	U7.W23	J21.6
FPGA_GPIO15	U7.W24	J21.8
FPGA_GPIO16	U7.W25	J21.10
FPGA_GPIO17	U7.W27	J21.12
FPGA_GPIO18	U7.W28	J21.14
FPGA_GPIO19	U7.V26	J21.16
FPGA_GPIO20	U7.V27	J21.17
FPGA_GPIO21	U7.AB25	J21.18

14 LED Indicators

The DNMEG_ARM_TILE (REV2) provides various LED's to indicate that status of the board.

14.1 User LED's

32 green LED's are provided to the user as a design aid during debugging. The LED's can be turned ON by driving the corresponding pin LOW. Table 9 describes the user LED's and their associated pin assignments on the FPGA (U7).

Table 9 – User LED's

Signal Name	FPGA Pin	LED
FPGA_LED0	U7.AH29	DS10
FPGA_LED1	U7.AH30	DS12
FPGA_LED2	U7.AG27	DS14
FPGA_LED3	U7.AG28	DS16
FPGA_LED4	U7.AG29	DS18
FPGA_LED5	U7.AG30	DS20
FPGA_LED6	U7.AF29	DS22
FPGA_LED7	U7.AF30	DS24
FPGA_LED8	U7.AF27	DS26
FPGA_LED9	U7.AE26	DS28
FPGA_LED10	U7.AE28	DS30
FPGA_LED11	U7.AE29	DS32
FPGA_LED12	U7.AD27	DS34

Signal Name	FPGA Pin	LED
FPGA_LED13	U7.AD28	DS36
FPGA_LED14	U7.AD29	DS38
FPGA_LED15	U7.AD30	DS40
FPGA_LED16	U7.AD25	DS42
FPGA_LED17	U7.AC24	DS44
FPGA_LED18	U7.AC25	DS46
FPGA_LED19	U7.AC26	DS29
FPGA_LED20	U7.AC27	DS31
FPGA_LED21	U7.AC28	DS33
FPGA_LED22	U7.AC29	DS35
FPGA_LED23	U7.AC30	DS37
FPGA_LED24	U7.AB26	DS39
FPGA_LED25	U7.AB27	DS41
FPGA_LED26	U7.AB29	DS43
FPGA_LED27	U7.AB30	DS45
FPGA_LED28	U7.AB23	DS21
FPGA_LED29	U7.AA22	DS23
FPGA_LED30	U7.AA24	DS25
FPGA_LED31	U7.AA25	DS27

14.2 Configuration DONE LED

After the FPGA has received all the configuration data successfully, it releases the DONE pin, which is pulled high by a pull-up resistor. A low-to-high transition on the DONE indicates configuration is complete and initialization of the device can begin. DONE pin drives a NFET and turns ON the blue LED (DS17) when the DONE pin goes high. Table 10 describes the DONE LED and its associated pin assignment on the FPGA (U21).

Table 10 – FPGA_DONE LED

Signal Name	FPGA Pin	LED
FPGA_DONE	U7.AJ28	DS7

14.3 Power Supply Status LED's

LED's are provided to indicate the presence of various power supplies. The power monitors (U15, U16) monitor the P12VD, P3.3VD, P3.0VD, P2.5VD, and P1.2VD voltage levels and signals an under-voltage condition by pulling "FPGA_PROG_N"

signal low. The status of this signal is indicated by DS19. Table 11 describes the power supply status LED's and their associated voltage source.

Table 11 – Power Supply Status LED's

Signal Name	Source	LED
P12VD	J5.1	DS4
P5VD	J5.4	DS3
P3.3VD	PSU5.6	DS2
P2.5VD	PSU2.6	DS6
PVDDIO	J4.2 (PSU1.6 or PSU3.6)	DS5
FPGA_PROG_N	U15.4, U16.4	DS19

15 Memory

15.1 SRAM

The 32-bit wide SRAM has the following connections to the Spartan FPGA. The SRAM shares its address and data bus with the FLASH – this requires that transactions to the SRAM and FLASH be mutually exclusive. Some address bits may not be used on the SRAM – check stuffing options for actual address width. Signal descriptions and functionality can be found in the datasheet distributed with this document.

Table 12 – SRAM Connections

Signal Name	FPGA Pin
SRAM_ADSC_N	U7.AD15
SRAM_ADSP_N	U7.AE15
SRAM_ADV_N	U7.AE6
SRAM_BWA_N	U7.AH8
SRAM_BWB_N	U7.AA11
SRAM_BWC_N	U7.AA15
SRAM_BWD_N	U7.AB10
SRAM_BWE_N	U7.AG8
SRAM_CE1_N	U7.AG15
SRAM_CE2	U7.AC8
SRAM_CE3_N	U7.AD8
SRAM_CLK	U7.AJ7
SRAM_DQ16	U7.AK12
SRAM_DQ17	U7.AA12
SRAM_DQ18	U7.AA13
SRAM_DQ19	U7.AB13
SRAM_DQ20	U7.AC13

Signal Name	FPGA Pin
SRAM_DQ21	U7.AF13
SRAM_DQ22	U7.AG13
SRAM_DQ23	U7.AJ13
SRAM_DQ24	U7.AA14
SRAM_DQ25	U7.AB14
SRAM_DQ26	U7.AE13
SRAM_DQ27	U7.AE14
SRAM_DQ28	U7.AH14
SRAM_DQ29	U7.AJ14
SRAM_DQ30	U7.AB15
SRAM_DQ31	U7.AC15
SRAM_DQP0	U7.AJ5
SRAM_DQP1	U7.AH7
SRAM_DQP2	U7.AJ12
SRAM_DQP3	U7.AK13
SRAM_FLASH_A0	U7.AE9
SRAM_FLASH_A1	U7.AE10
SRAM_FLASH_A10	U7.AJ11
SRAM_FLASH_A11	U7.AK11
SRAM_FLASH_A12	U7.AC11
SRAM_FLASH_A13	U7.AB12
SRAM_FLASH_A14	U7.AC12
SRAM_FLASH_A15	U7.AD12
SRAM_FLASH_A16	U7.AE12
SRAM_FLASH_A17	U7.AF12
SRAM_FLASH_A18	U7.AG12
SRAM_FLASH_A19	U7.AH12
SRAM_FLASH_A2	U7.AH10
SRAM_FLASH_A20	U7.AH4
SRAM_FLASH_A21	U7.AK15
SRAM_FLASH_A3	U7.AJ10
SRAM_FLASH_A4	U7.AD10
SRAM_FLASH_A5	U7.AD11
SRAM_FLASH_A6	U7.AE11
SRAM_FLASH_A7	U7.AF11
SRAM_FLASH_A8	U7.AG11
SRAM_FLASH_A9	U7.AH11
SRAM_FLASH_DQ0	U7.AK5
SRAM_FLASH_DQ1	U7.AG5
SRAM_FLASH_DQ10	U7.AB9
SRAM_FLASH_DQ11	U7.AC9
SRAM_FLASH_DQ12	U7.AF9

Signal Name	FPGA Pin
SRAM_FLASH_DQ13	U7.AG9
SRAM_FLASH_DQ14	U7.AJ9
SRAM_FLASH_DQ15	U7.AK9
SRAM_FLASH_DQ2	U7.AF6
SRAM_FLASH_DQ3	U7.AH6
SRAM_FLASH_DQ4	U7.AJ6
SRAM_FLASH_DQ5	U7.AD7
SRAM_FLASH_DQ6	U7.AE7
SRAM_FLASH_DQ7	U7.AG7
SRAM_FLASH_DQ8	U7.AJ8
SRAM_FLASH_DQ9	U7.AK8
SRAM_MODE	U7.AD14
SRAM_OE_N	U7.AE8
SRAM_WE_N	U7.AF8
SRAM_ZZ	U7.AD16

15.2 DRAM

The DNMEG_ARM_TILE (REV2) uses two 16-bit wide DRAM chips in parallel to create a 32-bit wide DRAM interface. The connections to the DRAM are listed below. Some address bits may not be used on the DRAM – check stuffing options for actual address width. Signal descriptions and functionality can be found in the datasheet distributed with this document.

Table 13 – DRAM Connections

Signal Name	FPGA Pin
DRAM_A0	U7.AK27
DRAM_A1	U7.AJ27
DRAM_A10	U7.AH23
DRAM_A11	U7.AG23
DRAM_A12	U7.AK23
DRAM_A2	U7.AK26
DRAM_A3	U7.AJ26
DRAM_A4	U7.AF25
DRAM_A5	U7.AG26
DRAM_A6	U7.AC23
DRAM_A7	U7.AD24
DRAM_A8	U7.AF23
DRAM_A9	U7.AE23
DRAM_BA0	U7.AJ23
DRAM_BA1	U7.AC22

Signal Name	FPGA Pin
DRAM_CAS_N	U7.AA19
DRAM_CKE	U7.AG20
DRAM_CLK0	U7.AK20
DRAM_CLK1	U7.AJ20
DRAM_CS_N	U7.AC19
DRAM_DQ0	U7.AB22
DRAM_DQ1	U7.AG22
DRAM_DQ10	U7.AB21
DRAM_DQ11	U7.AD20
DRAM_DQ12	U7.AC20
DRAM_DQ13	U7.AF20
DRAM_DQ14	U7.AE20
DRAM_DQ15	U7.AH20
DRAM_DQ16	U7.AK19
DRAM_DQ17	U7.AJ19
DRAM_DQ18	U7.AC18
DRAM_DQ19	U7.AB18
DRAM_DQ2	U7.AF22
DRAM_DQ20	U7.AF18
DRAM_DQ21	U7.AE18
DRAM_DQ22	U7.AK18
DRAM_DQ23	U7.AJ18
DRAM_DQ24	U7.AB17
DRAM_DQ25	U7.AA17
DRAM_DQ26	U7.AE17
DRAM_DQ27	U7.AJ17
DRAM_DQ28	U7.AH17
DRAM_DQ29	U7.AC16
DRAM_DQ3	U7.AK22
DRAM_DQ30	U7.AB16
DRAM_DQ31	U7.AE16
DRAM_DQ4	U7.AJ22
DRAM_DQ5	U7.AE21
DRAM_DQ6	U7.AD21
DRAM_DQ7	U7.AJ21
DRAM_DQ8	U7.AH21
DRAM_DQ9	U7.AA20
DRAM_DQM0	U7.AF19
DRAM_DQM1	U7.AE19
DRAM_DQM2	U7.AH19
DRAM_DQM3	U7.AG19
DRAM_RAS_N	U7.AD19

Signal Name	FPGA Pin
DRAM_WE_N	U7.AB19

15.3 FLASH

The FLASH w/ 16-bit wide data has the following connections to the Spartan FPGA. The FLASH can be given a 32-bit wide interface in RTL, requiring multiple reads/writes per transaction. The FLASH shares its address and data bus with the SRAM – this requires that transactions to the SRAM and FLASH be mutually exclusive. Some address bits may not be used on the FLASH – check stuffing options for actual address width. Signal descriptions and functionality can be found in the datasheet distributed with this document.

Table 14 – FLASH Connections

Signal Name	FPGA Pin
FLASH_CE_N	U7.AJ25
FLASH_OE_N	U7.AH25
FLASH_RESET_N	U7.AH24
FLASH_WE_N	U7.AE24
FLASH_WP_N	U7.AE25
SRAM_FLASH_A0	U7.AE9
SRAM_FLASH_A1	U7.AE10
SRAM_FLASH_A10	U7.AJ11
SRAM_FLASH_A11	U7.AK11
SRAM_FLASH_A12	U7.AC11
SRAM_FLASH_A13	U7.AB12
SRAM_FLASH_A14	U7.AC12
SRAM_FLASH_A15	U7.AD12
SRAM_FLASH_A16	U7.AE12
SRAM_FLASH_A17	U7.AF12
SRAM_FLASH_A18	U7.AG12
SRAM_FLASH_A19	U7.AH12
SRAM_FLASH_A2	U7.AH10
SRAM_FLASH_A20	U7.AH4
SRAM_FLASH_A21	U7.AK15
SRAM_FLASH_A3	U7.AJ10
SRAM_FLASH_A4	U7.AD10
SRAM_FLASH_A5	U7.AD11
SRAM_FLASH_A6	U7.AE11
SRAM_FLASH_A7	U7.AF11
SRAM_FLASH_A8	U7.AG11
SRAM_FLASH_A9	U7.AH11

Signal Name	FPGA Pin
SRAM_FLASH_DQ0	U7.AK5
SRAM_FLASH_DQ1	U7.AG5
SRAM_FLASH_DQ10	U7.AB9
SRAM_FLASH_DQ11	U7.AC9
SRAM_FLASH_DQ12	U7.AF9
SRAM_FLASH_DQ13	U7.AG9
SRAM_FLASH_DQ14	U7.AJ9
SRAM_FLASH_DQ15	U7.AK9
SRAM_FLASH_DQ2	U7.AF6
SRAM_FLASH_DQ3	U7.AH6
SRAM_FLASH_DQ4	U7.AJ6
SRAM_FLASH_DQ5	U7.AD7
SRAM_FLASH_DQ6	U7.AE7
SRAM_FLASH_DQ7	U7.AG7
SRAM_FLASH_DQ8	U7.AJ8
SRAM_FLASH_DQ9	U7.AK8

16 PS/2 Keyboard and Mouse

The PS/2 interface consists of a bidirectional clock and a single bidirectional data signal. Please see the Schematic Errata for the actual circuit used in production. The signal connections are listed below.

Table 15 – PS/2 Connections

Signal Name	FPGA Pin
KEYBOARD_CK	U7.AG24
KEYBOARD_TX	U7.AK24
MOUSE_CK	U7.AA16
MOUSE_TX	U7.AA18

17 AC97

The on-board AC97 SoundMAX® Codec has two 3.5mm audio jacks (J29 and J30) for input/output to the chip. There are also multiple testpoints that can be connected manually by the user to an external source for inputs/outputs to the chip other than those provided. Please consult the AC97 specification for a complete description of the functionality of the codec.

Table 16 – AC97 Connections

Signal Name	Pin

Signal Name	Pin
AUDIO_BIT_CLK	U7.AE22
AUDIO_RESET	U7.AK28
AUDIO_SDATA_IN	U7.AF16
AUDIO_SDATA_OUT	U7.AG18
AUDIO_SYNC	U7.AH27
LINE_OUT_R	J30.3
LINE_OUT_L	J30.2
MIC_IN	J29.2

In addition, several static signals are attached to DIP Switch S3. When the switches are in the OFF position, the signals will be HIGH. Turning the switches ON results in making the signals LOW.

Table 17 – Signals on S3

Signal Name	Pin
AUDIO_MODE	S3.8
AUDIO_CS0	S3.7
AUDIO_CS1	S3.6
AUDIO_EAPD	S3.5

18 RS232 Port

An RS232 serial port is provided for low speed communication with the application on the FPGA. The RS-232 standard specifies output voltage levels between –5V to –15V for logical 1 and +5V to +15V for logical 0. Input must be compatible with voltages in the range of -3V to -15V for logical 1 and +3V to +15V for logical 0. This ensures data bits are read correctly even at maximum cable lengths between DTE and DCE, specified as 50 feet.

The connections between the FPGA and the RS232 Port are shown below

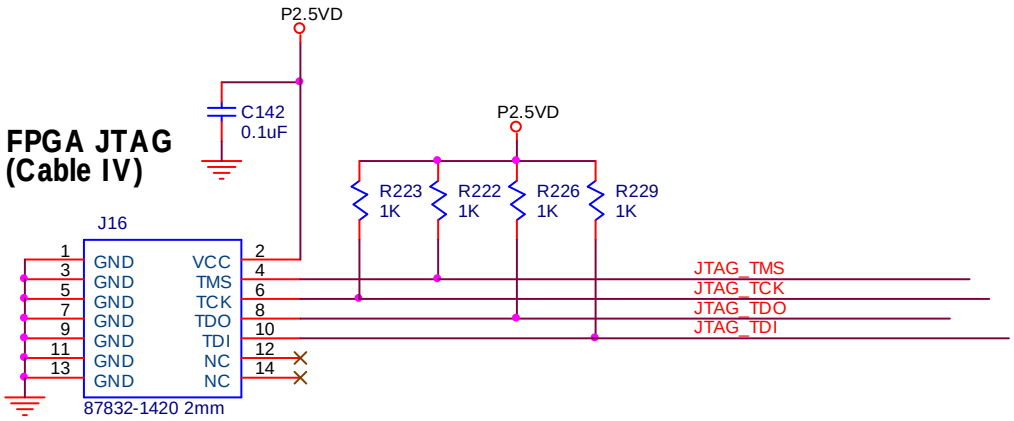
Table 18 - Connections between FPGA and the RS232 Port

Signal Name	FPGA Pin
FPGA_RXD	U7.K17
FPGA_TXD	U7.K18
RS232_EN_N	U7.A18

19 JTAG

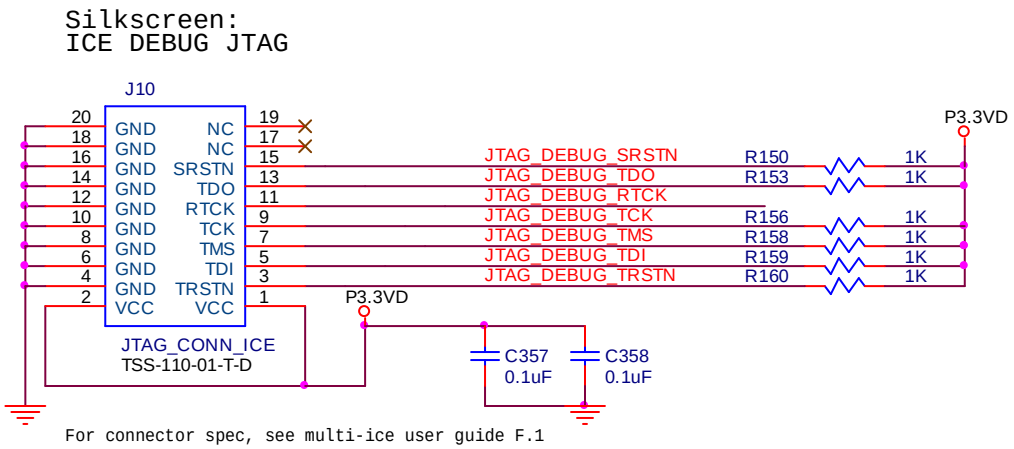
There are several JTAG connections on the DNMEG_ARM_TILE (REV2). The first of these connections, the Xilinx JTAG Header J16, allows for programming the Spartan 3 FPGA and the Xilinx PROM on the DNMEG_ARM_TILE (REV2).

Figure 4 – Xilinx JTAG Connector



J10 is the JTAG connector on the board for connecting an ARM debugger/emulator to the ARM Core Tile. Note: for J10 to be active, the signal ZHEADER_CFG_EN_N attached to the Spartan FPGA must be held HIGH.

Figure 5 – Multi-ICE JTAG Connector



The final two JTAG connectors, J12 and J13, are for reconfiguring devices on the ARM Core Tile. Both Xilinx- and Multi-ICE-style connectors are provided for this function, since there are both Xilinx and non-Xilinx parts in the JTAG chain on the Arm Core Tile. Note: for J12 and J13 to be active, the signal ZHEADER_CFG_EN_N attached to the Spartan FPGA must be held LOW.

More detail about the JTAG chains on the ARM Core Tile can be found in the documentation provided with the Core Tile.

20 Daughter Card Headers

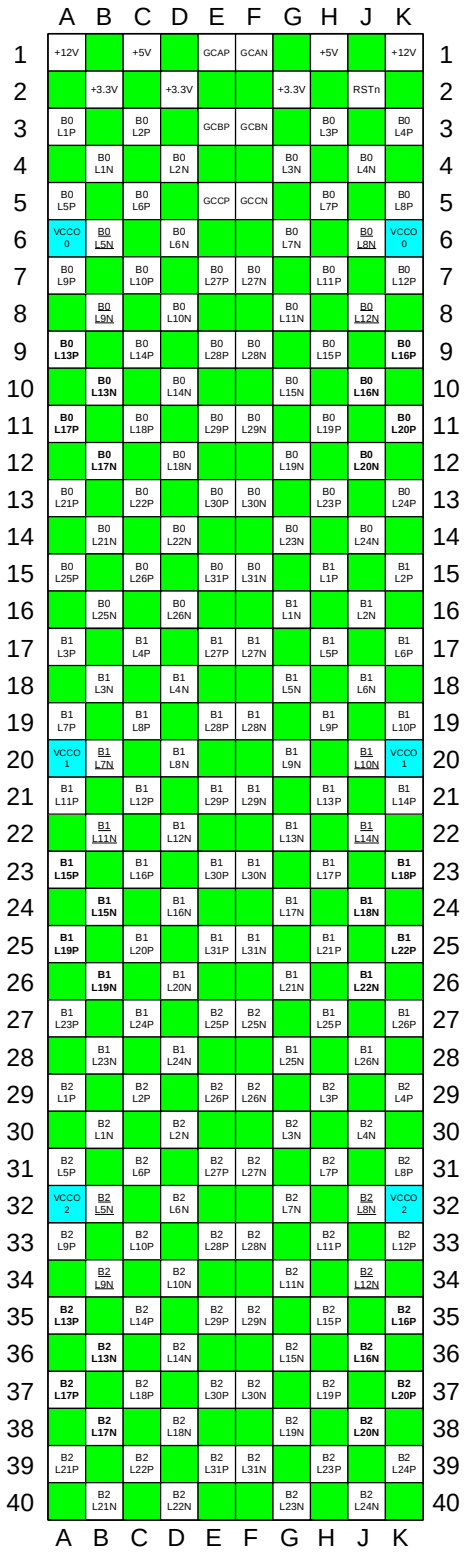
The DNMEG_ARM_TILE (REV2) has one 400-pin MEG-Array daughter card header (P1). All signals on the DNMEG_ARM_TILE (REV2) Daughter Card Headers are all routed as differential, 50-Ohm transmission lines. No length-matching is done on the PCB for Daughter Card signals, (except within a differential pair) because the Virtex-5 is capable of variable-delay input using the built-in Input/Output Delay Element (IODELAY) capabilities. Other connections on the daughter card connector system include three dedicated, differential clock connections for inputting global clocks from an external source, power connections, bank V_{CCO} power, and a reset signal.

20.1 Daughter Card clocking

Refer to the Clocking Chapter in this User Manual.

20.2 Daughter Card Header Pin Assignments

The pin assignments of the DNMEG_ARM_TILE (REV2) Daughter Card Headers were designed to reduce cross talk to manageable levels while operating at full speed of the Virtex-5 LVDS standards. The Daughter Card Header is divided into three banks, refer to the following figure.



	A	B	C	D	E	F	G	H	J	K	
1	+12V		+5V		GCAP	GCAN		+5V		+12V	1
2		+3.3V		+3.3V			+3.3V		RSTn		2
3	B0 L1P		B0 L2P		GCBP	GCBN		B0 L3P		B0 L4P	3
4		B0 L1N		B0 L2N			B0 L3N		B0 L4N		4
5	B0 L5P		B0 L6P		GCCP	GCCN		B0 L7P		B0 L8P	5
6	VCCO 0	B0 L5N		B0 L6N			B0 L7N		B0 L8N	VCCO 0	6
7	B0 L9P		B0 L10P		B0 L27P	B0 L27N		B0 L11P		B0 L12P	7
8		B0 L9N		B0 L10N			B0 L11N		B0 L12N		8
9	**B0 L13P**		B0 L14P		B0 L28P	B0 L28N		B0 L15P		**B0 L16P**	9
10		**B0 L13N**		B0 L14N			B0 L15N		**B0 L16N**		10
11	**B0 L17P**		B0 L18P		B0 L29P	B0 L29N		B0 L19P		**B0 L20P**	11
12		**B0 L17N**		B0 L18N			B0 L19N		**B0 L20N**		12
13	B0 L21P		B0 L22P		B0 L30P	B0 L30N		B0 L23P		B0 L24P	13
14		B0 L21N		B0 L22N			B0 L23N		B0 L24N		14
15	B0 L25P		B0 L26P		B0 L31P	B0 L31N		B1 L1P		B1 L2P	15
16		B0 L25N		B0 L26N			B1 L1N		B1 L2N		16
17	B1 L3P		B1 L4P		B1 L27P	B1 L27N		B1 L5P		B1 L6P	17
18		B1 L3N		B1 L4N			B1 L5N		B1 L6N		18
19	B1 L7P		B1 L8P		B1 L28P	B1 L28N		B1 L9P		B1 L10P	19
20	VCCO 1	B1 L7N		B1 L8N			B1 L9N		B1 L10N	VCCO 1	20
21	B1 L11P		B1 L12P		B1 L29P	B1 L29N		B1 L13P		B1 L14P	21
22		B1 L11N		B1 L12N			B1 L13N		B1 L14N		22
23	**B1 L15P**		B1 L16P		B1 L30P	B1 L30N		B1 L17P		**B1 L18P**	23
24		**B1 L15N**		B1 L16N			B1 L17N		**B1 L18N**		24
25	**B1 L19P**		B1 L20P		B1 L31P	B1 L31N		B1 L21P		**B1 L22P**	25
26		**B1 L19N**		B1 L20N			B1 L21N		**B1 L22N**		26
27	B1 L23P		B1 L24P		B2 L25P	B2 L25N		B1 L25P		B1 L26P	27
28		B1 L23N		B1 L24N			B1 L25N		B1 L26N		28
29	B2 L1P		B2 L2P		B2 L26P	B2 L26N		B2 L3P		B2 L4P	29
30		B2 L1N		B2 L2N			B2 L3N		B2 L4N		30
31	B2 L5P		B2 L6P		B2 L27P	B2 L27N		B2 L7P		B2 L8P	31
32	VCCO 2	B2 L5N		B2 L6N			B2 L7N		B2 L8N	VCCO 2	32
33	B2 L9P		B2 L10P		B2 L28P	B2 L28N		B2 L11P		B2 L12P	33
34		B2 L9N		B2 L10N			B2 L11N		B2 L12N		34
35	**B2 L13P**		B2 L14P		B2 L29P	B2 L29N		B2 L15P		**B2 L16P**	35
36		**B2 L13N**		B2 L14N			B2 L15N		**B2 L16N**		36
37	**B2 L17P**		B2 L18P		B2 L30P	B2 L30N		B2 L19P		**B2 L20P**	37
38		**B2 L17N**		B2 L18N			B2 L19N		**B2 L20N**		38
39	B2 L21P		B2 L22P		B2 L31P	B2 L31N		B2 L23P		B2 L24P	39
40		B2 L21N		B2 L22N			B2 L23N		B2 L24N		40
	A	B	C	D	E	F	G	H	J	K	

Figure 6 - Daughter Card Header Pin Assignments

20.3 FPGA to Daughter Card Header IO Connections

Most connections to the Daughter Card Header come from the ARM X Header, which carries the signals for the AHB bus. The intention in the design was to provide direct access to the ARM Core Tile from a host board (not needing to route through an intermediary FPGA). While this is completely achieved, the Spartan is still necessary to drive some setup signals for correct ARM execution. The Ethernet connection on the DNMEG_ARM_TILE (REV2) is only available if the host board is connected – these signals are routed directly to the Meg-Array connector.

Table 19 - Daughter Card Header IO Connections

DC SIGNAL	SIGNAL	Daughter Card Receptacle
DC_B0L17N_CC	XHEADER_HRDATA1	P1.B12
DC_B0L17P_CC	XHEADER_HRDATA0	P1.A11
DC_B0L18N	XHEADER_HRDATA3	P1.D12
DC_B0L18P	XHEADER_HRDATA2	P1.C11
DC_B0L19N	XHEADER_HRDATA5	P1.G12
DC_B0L19P	XHEADER_HRDATA4	P1.H11
DC_B0L20N_CC	XHEADER_HRDATA7	P1.J12
DC_B0L20P_CC	XHEADER_HRDATA6	P1.K11
DC_B0L21N	XHEADER_HRDATA9	P1.B14
DC_B0L21P	XHEADER_HRDATA8	P1.A13
DC_B0L22N	XHEADER_HRDATA11	P1.D14
DC_B0L22P	XHEADER_HRDATA10	P1.C13
DC_B0L23N	XHEADER_HRDATA13	P1.G14
DC_B0L23P	XHEADER_HRDATA12	P1.H13
DC_B0L24N	XHEADER_HRDATA15	P1.J14
DC_B0L24P	XHEADER_HRDATA14	P1.K13
DC_B0L25N	XHEADER_HRDATA17	P1.B16
DC_B0L25P	XHEADER_HRDATA16	P1.A15
DC_B0L26N	XHEADER_HRDATA19	P1.D16
DC_B0L26P	XHEADER_HRDATA18	P1.C15
DC_B0L31N	XHEADER_HRDATA29	P1.F15
DC_B0L31P	XHEADER_HRDATA28	P1.E15
DC_B1L10N_VREF	XHEADER_HADDR12	P1.J20
DC_B1L10P	XHEADER_HADDR13	P1.K19
DC_B1L12N	XHEADER_HSIZE1	P1.D22
DC_B1L12P	XHEADER_HADDR9	P1.C21
DC_B1L13N	XHEADER_HADDR6	P1.G22
DC_B1L13P	XHEADER_HADDR7	P1.H21
DC_B1L14N_VREF	XHEADER_HADDR4	P1.J22
DC_B1L14P	XHEADER_HADDR5	P1.K21

DC SIGNAL	SIGNAL	Daughter Card Receptacle
DC_B1L17N	XHEADER_HDATA30	P1.G24
DC_B1L17P	XHEADER_HDATA31	P1.H23
DC_B1L18N_CC	XHEADER_HDATA28	P1.J24
DC_B1L18P_CC	XHEADER_HDATA29	P1.K23
DC_B1L1N	XHEADER_HADDR30	P1.G16
DC_B1L1P	XHEADER_HADDR31	P1.H15
DC_B1L21N	XHEADER_PLLLOCK	P1.G26
DC_B1L21P	XHEADER_ARM_PORESET_N	P1.H25
DC_B1L22N_CC	XHEADER_CONFIGINIT	P1.J26
DC_B1L22P_CC	XHEADER_HCLKIN_UP	P1.K25
DC_B1L25N	XHEADER_HLOCK	P1.G28
DC_B1L25P	XHEADER_HREADY	P1.H27
DC_B1L26N	XHEADER_HWRITE	P1.J28
DC_B1L26P	XHEADER_HBUSREQ	P1.K27
DC_B1L27N	XHEADER_HBURST1	P1.F17
DC_B1L27P	XHEADER_HRDATA30	P1.E17
DC_B1L29N	XHEADER_HSIZE2	P1.F21
DC_B1L29P	XHEADER_HBURST0	P1.E21
DC_B1L2N	XHEADER_HADDR28	P1.J16
DC_B1L2P	XHEADER_HADDR29	P1.K15
DC_B1L30N	XHEADER_HRDATA25	P1.F23
DC_B1L30P	XHEADER_HRDATA24	P1.E23
DC_B1L3N	XHEADER_HADDR26	P1.B18
DC_B1L3P	XHEADER_HADDR27	P1.A17
DC_B1L4N	XHEADER_HADDR24	P1.D18
DC_B1L4P	XHEADER_HADDR25	P1.C17
DC_B1L5N	XHEADER_HADDR22	P1.G18
DC_B1L5P	XHEADER_HADDR23	P1.H17
DC_B1L6N	XHEADER_HADDR20	P1.J18
DC_B1L6P	XHEADER_HADDR21	P1.K17
DC_B1L7N_VREF	XHEADER_HADDR18	P1.B20
DC_B1L7P	XHEADER_HADDR19	P1.A19
DC_B1L8N	XHEADER_HADDR16	P1.D20
DC_B1L8P	XHEADER_HADDR17	P1.C19
DC_B1L9N	XHEADER_HADDR14	P1.G20
DC_B1L9P	XHEADER_HADDR15	P1.H19
DC_B2L10N	XHEADER_HDATA1	P1.D34
DC_B2L10P	XHEADER_HDATA2	P1.C33
DC_B2L11N	XHEADER_HDATA20	P1.G34
DC_B2L11P	XHEADER_HDATA0	P1.H33

DC SIGNAL	SIGNAL	Daughter Card Receptacle
DC_B2L12N_VREF	XHEADER_HDATA18	P1.J34
DC_B2L12P	XHEADER_HDATA19	P1.K33
DC_B2L13N_CC	XHEADER_HDATA16	P1.B36
DC_B2L13P_CC	XHEADER_HDATA17	P1.A35
DC_B2L14N	XHEADER_HADDR10	P1.D36
DC_B2L14P	XHEADER_HADDR11	P1.C35
DC_B2L15N	XHEADER_HADDR2	P1.G36
DC_B2L15P	XHEADER_HADDR3	P1.H35
DC_B2L16N_CC	XHEADER_HADDR0	P1.J36
DC_B2L16P_CC	XHEADER_HADDR1	P1.K35
DC_B2L17N_CC	XHEADER_HBURST2	P1.B38
DC_B2L17P_CC	XHEADER_HRDATA31	P1.A37
DC_B2L18N	XHEADER_HRDATA21	P1.D38
DC_B2L18P	XHEADER_HRDATA20	P1.C37
DC_B2L19N	XHEADER_HRDATA23	P1.G38
DC_B2L19P	XHEADER_HRDATA22	P1.H37
DC_B2L1N	XHEADER_HDATA25	P1.B30
DC_B2L1P	XHEADER_HDATA26	P1.A29
DC_B2L20N_CC	XHEADER_HADDR8	P1.J38
DC_B2L20P_CC	XHEADER_HSIZE0	P1.K37
DC_B2L22N	XHEADER_HRDATA27	P1.D40
DC_B2L22P	XHEADER_HRDATA26	P1.C39
DC_B2L23N	XHEADER_HTRANS0	P1.G40
DC_B2L23P	XHEADER_HTRANS1	P1.H39
DC_B2L24N	XHEADER_HGRANT	P1.J40
DC_B2L24P	XHEADER_HRESP0	P1.K39
DC_B2L26N	XHEADER_HDATA23	P1.F29
DC_B2L26P	XHEADER_HDATA24	P1.E29
DC_B2L27N	XHEADER_HDATA21	P1.F31
DC_B2L27P	XHEADER_HDATA22	P1.E31
DC_B2L28N	XHEADER_HPROT0	P1.F33
DC_B2L28P	XHEADER_HPROT1	P1.E33
DC_B2L29N	XHEADER_CONFIGRST_N	P1.F35
DC_B2L29P	XHEADER_RESET_N	P1.E35
DC_B2L30N	XHEADER_HRESP1	P1.F37
DC_B2L30P	XHEADER_HRESP2	P1.E37
DC_B2L3N	XHEADER_HDATA15	P1.G30
DC_B2L3P	XHEADER_HDATA27	P1.H29
DC_B2L4N	XHEADER_HDATA13	P1.J30
DC_B2L4P	XHEADER_HDATA14	P1.K29

DC SIGNAL	SIGNAL	Daughter Card Receptacle
DC_B2L5N_VREF	XHEADER_HDATA11	P1.B32
DC_B2L5P	XHEADER_HDATA12	P1.A31
DC_B2L6N	XHEADER_HDATA9	P1.D32
DC_B2L6P	XHEADER_HDATA10	P1.C31
DC_B2L7N	XHEADER_HDATA7	P1.G32
DC_B2L7P	XHEADER_HDATA8	P1.H31
DC_B2L8N_VREF	XHEADER_HDATA5	P1.J32
DC_B2L8P	XHEADER_HDATA6	P1.K31
DC_B2L9N_VREF	XHEADER_HDATA3	P1.B34
DC_B2L9P	XHEADER_HDATA4	P1.A33
DC_rB1L28N	ETHB_MDC	P1.F19
DC_rB1L28P	ETHB_MDIO	P1.E19
DC_VCCO0_1	PVDDIO	P1.A6
DC_VCCO0_2	PVDDIO	P1.K6
DC_VCCO1_1	PVDDIO	P1.A20
DC_VCCO1_2	PVDDIO	P1.K20
DC_VCCO2_1	PVDDIO	P1.A32
DC_VCCO2_2	PVDDIO	P1.K32
DC_xB0L10N	XHEADER_HPROT2	P1.D8
DC_xB0L10P	XHEADER_HPROT3	P1.C7
DC_xB0L11N	HOST_SPARTAN_IC4	P1.G8
DC_xB0L11P	HOST_SPARTAN_IC3	P1.H7
DC_xB0L12N_VREF	HOST_SPARTAN_IC6	P1.J8
DC_xB0L12P	HOST_SPARTAN_IC5	P1.K7
DC_xB0L13N_CC	HOST_SPARTAN_IC8	P1.B10
DC_xB0L13P_CC	HOST_SPARTAN_IC7	P1.A9
DC_xB0L14N	HOST_SPARTAN_IC10	P1.D10
DC_xB0L14P	HOST_SPARTAN_IC9	P1.C9
DC_xB0L15N	HOST_SPARTAN_IC12	P1.G10
DC_xB0L15P	HOST_SPARTAN_IC11	P1.H9
DC_xB0L16N_CC	HOST_SPARTAN_IC14	P1.J10
DC_xB0L16P_CC	HOST_SPARTAN_IC13	P1.K9
DC_xB0L1N_SDA	XHEADER_FIQ_N	P1.B4
DC_xB0L1P_SCL	XHEADER_IRQ_N	P1.A3
DC_xB0L2N	HOST_SPARTAN_IC15	P1.D4
DC_xB0L2P	XHEADER_BIGENDOUT	P1.C3
DC_xB0L3N	HOST_SPARTAN_IC25	P1.G4
DC_xB0L3P	HOST_SPARTAN_IC16	P1.H3
DC_xB0L4N	HOST_SPARTAN_IC27	P1.J4
DC_xB0L4P	HOST_SPARTAN_IC26	P1.K3

DC SIGNAL	SIGNAL	Daughter Card Receptacle
DC_xB0L5N_VREF	not connected	P1.B6
DC_xB0L5P	HOST_SPARTAN_IC28	P1.A5
DC_xB0L6N	HOST_SPARTAN_IC2	P1.D6
DC_xB0L6P	not connected	P1.C5
DC_xB0L7N	XHEADER_HPROT4	P1.G6
DC_xB0L7P	XHEADER_HPROT5	P1.H5
DC_xB0L8N_VREF	XHEADER_HPROT2	P1.J6
DC_xB0L8P	XHEADER_HPROT3	P1.K5
DC_xB0L9N_VREF	XHEADER_HPROT4	P1.B8
DC_xB0L9P	XHEADER_HPROT5	P1.A7
DC_xB1L11N_VREF	not connected	P1.B22
DC_xB1L11P	not connected	P1.A21
DC_xB1L15N_CC	not connected	P1.B24
DC_xB1L15P_CC	not connected	P1.A23
DC_xB1L16N	not connected	P1.D24
DC_xB1L16P	not connected	P1.C23
DC_xB1L19N_CC	HOST_SPARTAN_IC18	P1.B26
DC_xB1L19P_CC	HOST_SPARTAN_IC17	P1.A25
DC_xB1L20N	HOST_SPARTAN_IC20	P1.D26
DC_xB1L20P	HOST_SPARTAN_IC19	P1.C25
DC_xB1L23N	HOST_SPARTAN_IC22	P1.B28
DC_xB1L23P	HOST_SPARTAN_IC21	P1.A27
DC_xB1L24N	HOST_SPARTAN_IC24	P1.D28
DC_xB1L24P	HOST_SPARTAN_IC23	P1.C27
DC_xB2L2N	HOST_SPARTAN_IC1	P1.D30
DC_xB2L2P	HOST_SPARTAN_IC0	P1.C29
DC_xzrB2L31N	not connected	P1.F39
DC_xzrB2L31P	CLK125_ETHB_25	P1.E39
DC_zB0L27N	ETHB_RXD1	P1.F7
DC_zB0L27P	ETHB_RXD0	P1.E7
DC_zB0L28N	ETHB_RXD3	P1.F9
DC_zB0L28P	ETHB_RXD2	P1.E9
DC_zB0L29N	ETHB_TXD2	P1.F11
DC_zB0L29P	ETHB_TXD1	P1.E11
DC_zB0L30N	ETHB_RX_CTL	P1.F13
DC_zB0L30P	ETHB_TXD3	P1.E13

20.4 Power and Reset

The +3.3V, +5V and +12V power rails are supplied to the DNMEG_ARM_TILE (REV2) Daughter Card Headers from the host Dini Card, e.g. DN9000K10. Each pin on the MEG-Array connector is rated to tolerate 1A of current without thermal overload. Each power rail supplied from the Daughter Card Header is fused to prevent damage from overload. The preferred power source is the ATX connector (J5) and not the power pins on the MEG-Array

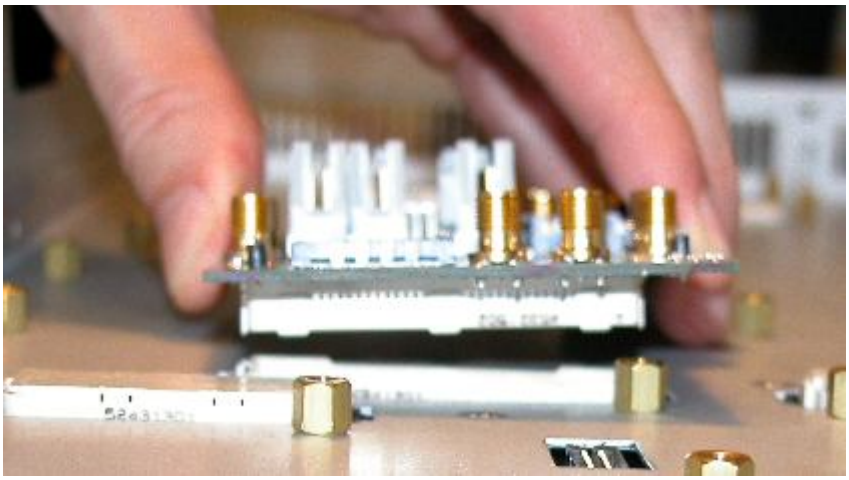
The "DC_RST_N" signal is pulled up on the DNMEG_ARM_TILE (REV2) Daughter Card. The signal is also routed to the FPGA (U7) and can be used as a reset to the logic, refer to Table 20.

Table 20 – Daughter Card Reset Signal (DC_RST_N)

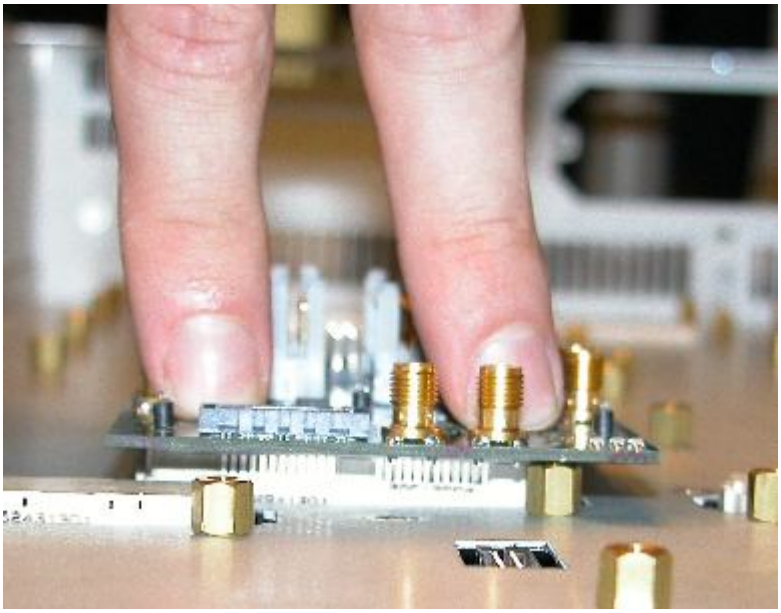
Signal Name	FPGA
DC_RST_N	U7.V2

20.5 Insertion/Removal of Daughter Card

Due to the high density MEG-Array connectors, the pins on the plug and receptacle of the MEG-Array connectors are very delicate. When plugging in a daughter card, make sure to align the daughter card first before pressing on the connector. *Be absolutely certain that both the small and the large keys at the narrow ends of the MEG-Array headers line up BEFORE applying pressure to mate the connectors!*



Place it down flat, then press down gently.



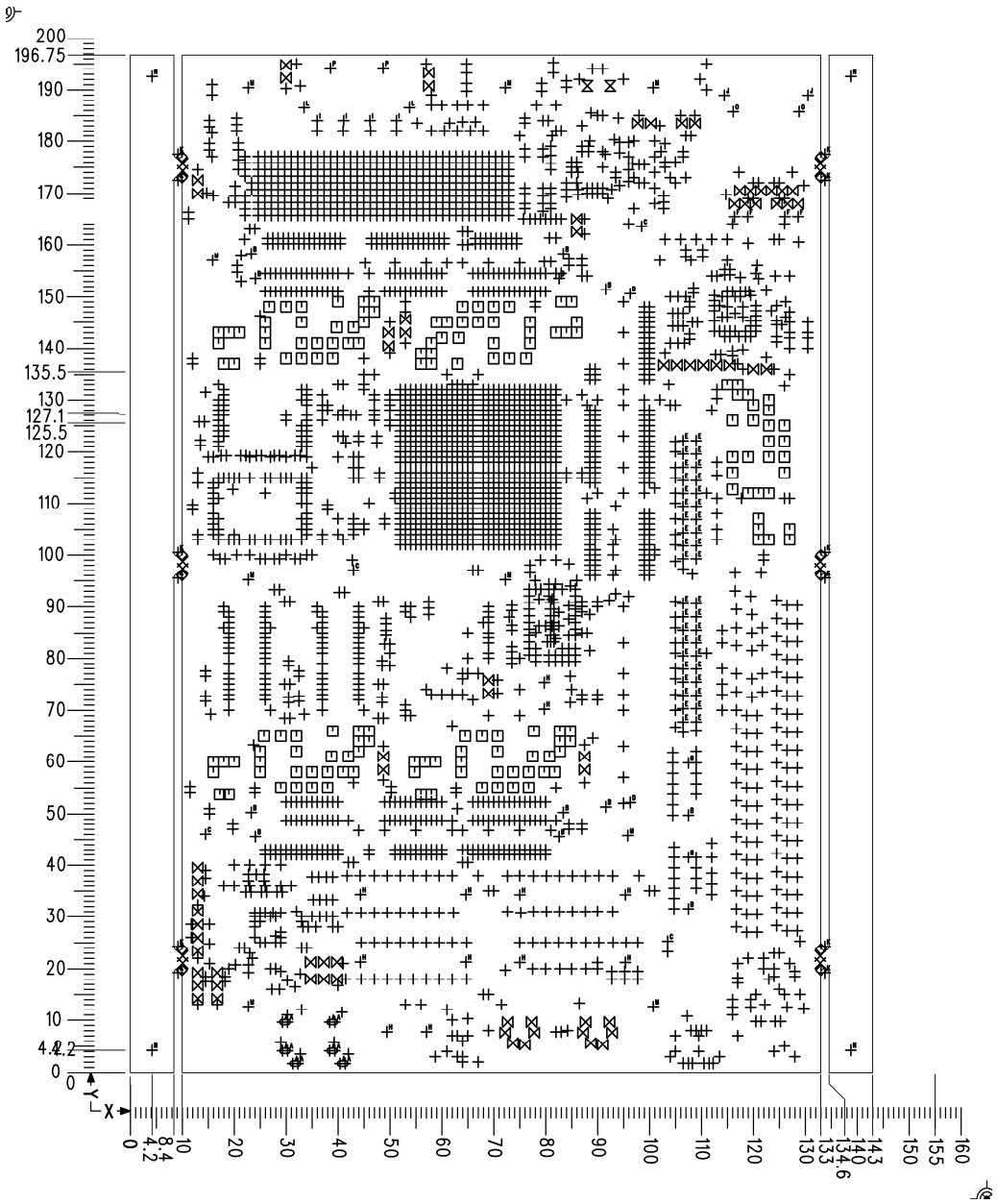
20.6 MEG Array Specifications

Manufacturer	FCI
Part Number	74390-101LF – Bottom Receptacle (P2) 84520-102LF – Top Plug (P1)
RoHS Lead Free Compatible	yes
Total Number Of Positions	400
Contact Area Plating	0.76 μm (30 μin.) gold over 0.76 μm (30 μin.) nickel
Mating Force	30 grams per contact average
Unmating Force	20 grams per contact average
Insulation Resistance	1000 M ohms
Withstanding Voltage	200 VAC
Current Rating	0.45 amps
Contact Resistance	20 to 25 m ohms max (initial), 10 m ohms max increase (after testing)
Temperature Range	-40 °C to +85 °C
Trademark	MEG-Array®
Approvals and Certification	UL and CSA approved
Product Specification	GSe -12-100, from FCI website
Pick-up Cap	yes
Housing Material	LCP
Contact Material	Copper Alloy
Durability (Mating Cycles)	50

21 Mechanical

21.1 Dimensions

The DNMEG_ARM_TILE (REV2) Daughter Card measures 133mm x 196.75mm.



Chapter 5

Appendix

22 Appendix A: UCF File

See the CUSTOMER CD for the Xilinx Universal Constraint File (UCF) file.

23 Appendix B: Using a Third-Party ARM Debugger

ARM debuggers are extremely useful for the development of ARM applications, and the DNMEG_ARM_TILE (REV2) supports a wide range of third-party debuggers through the DEBUG JTAG interface (see section 19). To successfully use such a debugger, the DEBUG path must be present and enabled. Make sure the following signals are configured correctly.

Signal Name	Attached To…	Value	Purpose
XHEADER_DBGEN	S2.4	HIGH	Enable debugging on ARM Chip
ZHEADER_CFGEN_N	U7.J17	HIGH	Disable CONFIG JTAG path / Enable DEBUG JTAG path
ZHEADER_RTCKEN_N	U7.	LOW	Enable RTCK on DEBUG JTAG interface

Also consider the speed of the JTAG clock. Please consult the documentation for your ARM Test Chip and your debugger interface for specific timings and compatibility; as a rule of thumb, lower JTAG clock speeds are preferred for best compatibility. Testing has shown the DEBUG interface to run reliably at 3MHz.